

PIEZOELECTRICALLY-TRANSDUCED SILICON MICROMECHANICAL RESONATORS

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PIEZOELECTRICALLY-TRANSDUCED SILICON MICROMECHANICAL RESONATORS

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SUMMARY

This thesis reports on the design and fabrication of micro-electro-mechanical (MEM) resonators on silicon that are piezoelectrically-transduced for operation in the very high frequency (VHF) range. These devices have a block-type or beam-type design, and are designed to resonate in their in-plane and out-of-plane bulk extensional modes. Two piezoelectric materials were taken into consideration, zinc-oxide (ZnO) and lead-zirconate-titanate (PZT). The resonators are fabricated on silicon-on-insulator (SOI) wafers and the metal/piezo/metal stack of layers forming the device is built and patterned on the device layer silicon via photolithography techniques, RF sputtering (for the piezo-layer) and electron-beam evaporation (for the metal layers). The designing aspect involved ANSYS simulations of the mode-shapes and estimation of frequencies, and these have correlated well with experimental results. Devices with RF sputtered ZnO were successfully fabricated and tested to give high quality factors at reasonably high frequencies. A gold ground plane was implemented to reduce the feed-through level and increase the signal-to-noise ratio. Extensive characterization of PZT was also done as a replacement for ZnO, as the former material has a much higher piezoelectric coefficient (~20X that of ZnO) and can therefore extend the operation of these MEM resonators into the UHF range. Although the basic design of the device remains the same, incorporation of PZT complicates the process flow considerably with respect to the chemistry now involved with the patterning of different layers. The frequency response for ZnO-based resonators as well as all the characterization data for PZT has been reported.

CHAPTER 1

INTRODUCTION

The technology thrusts driving all the research in wireless telecommunication devices has been miniaturization and added functionality. The use of bulky off-chip frequency selective components in current wireless devices makes their fabrication and packaging that much more complicated and cumbersome. Radio frequency micro-electro-mechanical-systems, or RF MEMS, has emerged as an extremely potent technology to cater to all the requirements of future mobile communication handsets.

RF MEMS comprise of high quality-factor inductors, tunable capacitors, high-value resistors, tunable filters and resonators. The primary advantage of this technology is that it can be incorporated on-chip using the same set of equipment required for conventional integrated chip (IC) fabrication, such as photolithography tools, reactive ion etchers (RIE), inductively-coupled plasma (ICP) etchers, RF and DC sputtering tools for deposition of dielectrics and metals, to name a few. The central microprocessor in the wireless device of the future will consist of two modules: the first dealing with CMOS circuitry and the second having all the RF MEMS components, allowing for very high density integration on silicon, thus bringing about reduction in size and increased efficiency of operation.

Micro-electro-mechanical resonators are the primary components of tunable filters, besides having other specific applications as mass sensors in biological and chemical

environments. There are many methods of actuation and sensing of these resonators, as well as various designs specific to the final application. They can be actuated by the following means:

- Capacitive transduction: This involves the use of two parallel-plate capacitors for actuation and sensing. The electrodes are on either side of the resonating body, separated by an air gap. Resonance is achieved by varying the drive voltage to the input capacitor (between the input electrode and the body), which is then detected by the output capacitor (between the output electrode and the body). A schematic of a capacitive MEM resonator is given below in figure 1.1.

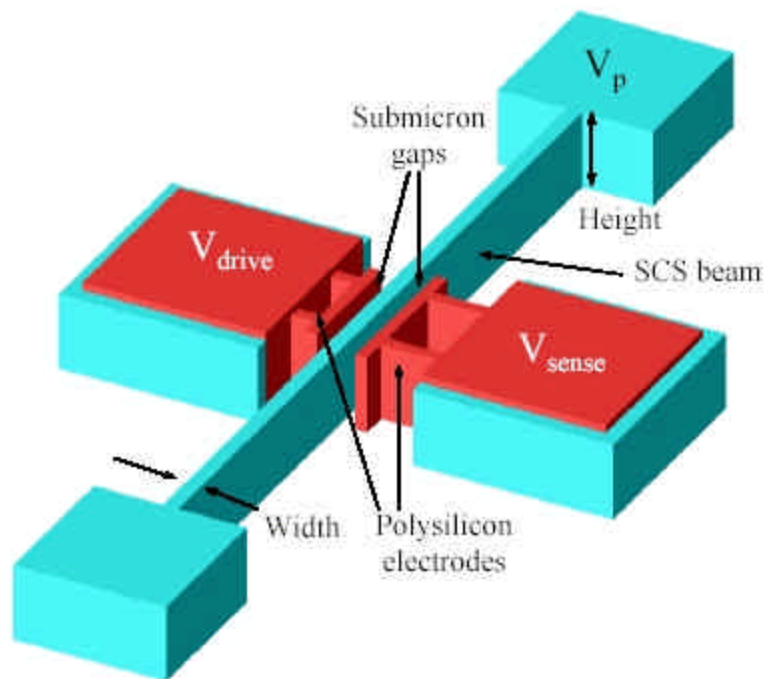


Fig. 1.1: Schematic of a capacitively-transduced resonator

- Piezoelectric transduction: In these resonators, both actuation and sensing are carried out by piezoelectric effects. The resonator body is formed by a metal/piezoelectric/metal stack of layers. When an alternating current is passed between the two metal electrodes on the drive side, the resultant electric field in the piezoelectric material causes it to change shape. Due to coupling between the piezoelectric layer and the single-crystalline silicon resonator body, resonance is achieved. This change in shape results in an electric field in the piezoelectric material on the sense side of the resonator. The resultant current is then picked up by the sense electrodes. A schematic of a clamped-clamped piezoelectric beam MEM resonator with ZnO as the piezoelectric material is given below in figure 1.2.

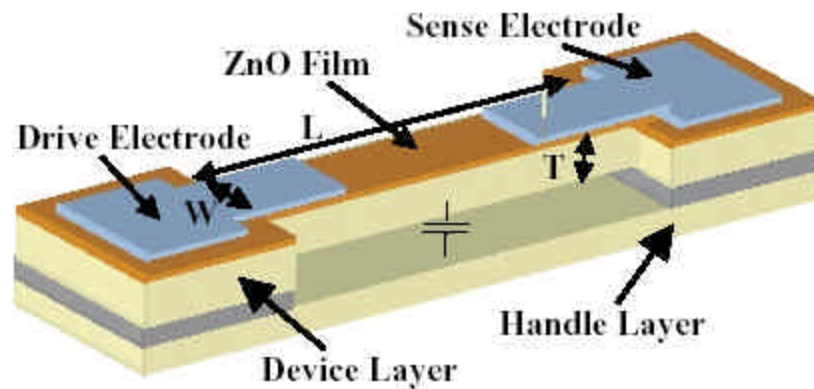


Fig. 1.2: Schematic of a piezoelectric beam resonator

- Other transduction means include magnetostrictive and thermal mechanisms. The former utilizes the property of magnetostrictive materials to change shape in a varying magnetic field, while thermal resonators involve the change in temperature for oscillation.

Capacitive and piezoelectric resonators are more attractive options, as they use the same mechanisms for actuation and sensing. The advantage of piezoelectric resonators is that they have very low motional impedances when compared to capacitive devices because the coupling between the input and the output is directly correlated to the piezoelectric properties of the material. Capacitive devices can have impedances in the range of Mega-ohms, whereas piezoelectric devices have it in the kilo-ohm (or less) range. This makes them suitable candidates when designing filters. To obtain low impedances for capacitive devices, extremely small gaps (in the nanometer-range) between the electrodes and the resonator body are required, thus complicating the fabrication process. However, since there is no contact between the electrodes and the body, the quality factors of these devices is much higher when compared to piezoelectric MEM resonators. Piezoelectric resonators are also easier to fabricate and take lesser time than capacitive ones. It can, therefore, be concluded that piezoelectric resonators are the better option for getting high frequency operation with reasonably high quality factors.

This thesis is divided into a number of sections. Chapter 1 introduces RF MEMS and compares different transduction mechanisms for MEM resonators, with specific preference given to piezoelectric transduction. Chapter 2 provides a brief literature review of the work that has been previously done in this field. Chapter 3 discusses the implementation strategies carried out during the course of the project, with all the characterization and fabrication aspects for both ZnO and PZT-based devices explained in detail. Chapter 4 provides the results from the ZnO-based devices. Finally, chapter 5 provides a conclusion and gives recommendations for future work in this area.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

In 1880, Jacques and Pierre Curie discovered an unusual characteristic of certain crystalline minerals: when subjected to a mechanical force, the crystals became electrically polarized. Tension and compression generated voltages of opposite polarity, and in proportion to the applied force. Subsequently, the converse of this relationship was confirmed: if one of these voltage-generating crystals was exposed to an electric field it lengthened or shortened according to the polarity of the field, and in proportion to the strength of the field. These behaviors were labeled the piezoelectric effect and the inverse piezoelectric effect, respectively, from the Greek word *piezein*, meaning to press or squeeze.

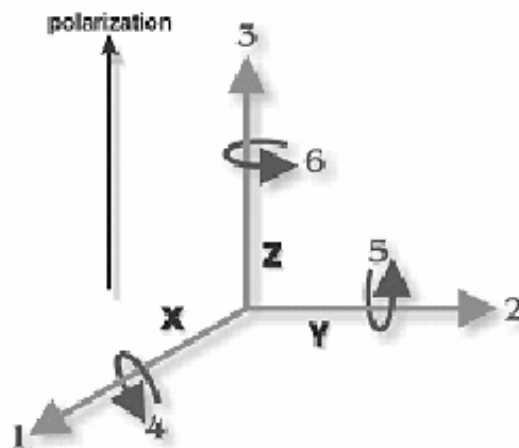


Fig. 2.1: The direction convention used to represent the piezoelectric coefficients

Some of the constants which are of prime importance are (refer to figure 2.1 above):

d_{33} = this is the induced polarization in direction 3 per unit stress applied in direction 3, or alternatively, it's the induced strain in direction 3 per unit electric field applied in direction 3.

d_{31} = this is the induced polarization in direction 3 per unit stress applied in direction 1, or alternatively, it's the induced strain in direction 3 per unit electric field applied in direction 1.

Both these constants have units of pico-Coulomb/Newton, or pico-meter/Volt.

2.2 ZINC OXIDE (ZnO)

Zinc oxide (ZnO) exhibits a wurtzite crystal structure, as shown in figure 2.2 below.

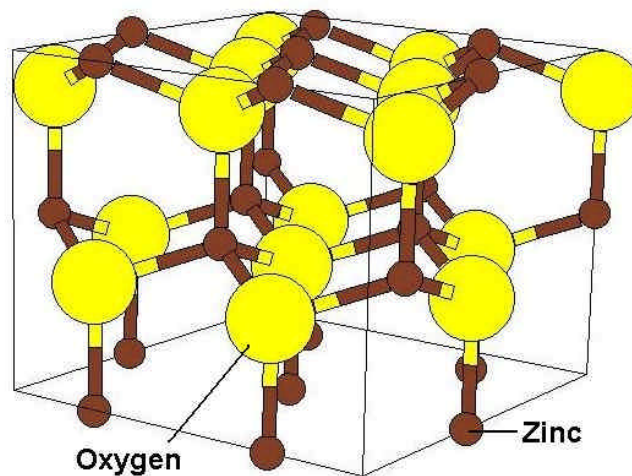


Fig. 2.2: Schematic of a ZnO unit cell showing the wurtzite-type crystal structure

Non-central symmetry and polar surfaces are characteristic of the wurtzite structure. The structure of ZnO has alternate planes of O^{2-} and Zn^{2+} ions along the c-axis. Due to the positively charged Zn polar surfaces and the negatively charged O polar surfaces, a resultant normal dipole moment is generated, making ZnO piezoelectric in nature along the c-axis.

2.3 LEAD-ZIRCONATE-TITANATE (PZT)

2.3.1 Piezoelectric actuation in PZT

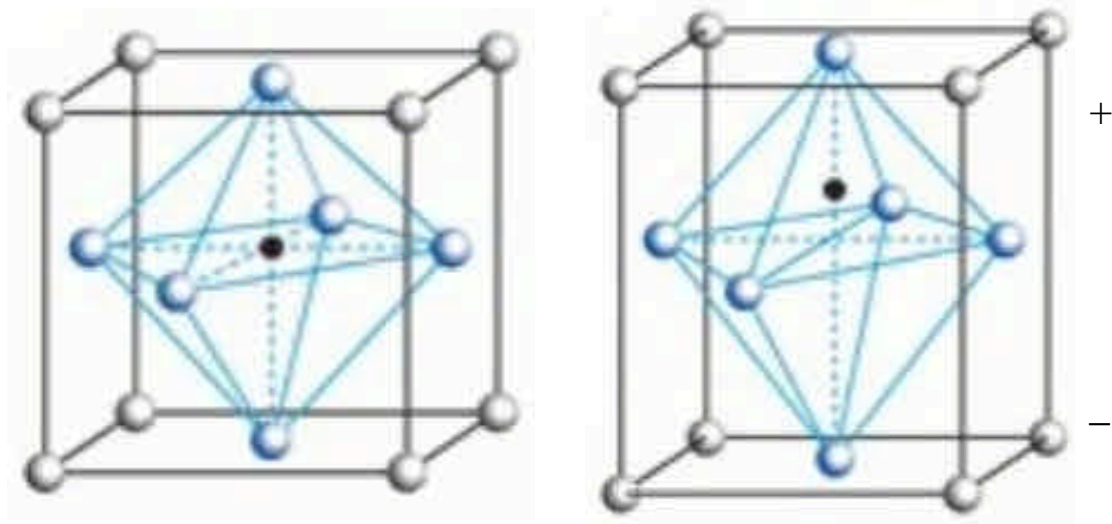


Fig. 2.3: The normal perovskite crystal structure of PZT above the Curie temperature (Left) (this is variable depending on the relative composition of Pb, Zr and Ti in the mixture); The tetragonal perovskite structure below the Curie temperature (Right)

Why is the crystal structure important? The crystal structure is what controls the piezoelectric actuation mechanism in PZT.

The crystal structure of lead-zirconate-titanate is shown in figure 2.3 above. Above the Curie temperature, PZT crystallites have a cubic structure and are, therefore, centrosymmetric (Figure 2.3, left). Centrosymmetric crystal structures are crystals that are symmetric along all axes through the center of the crystal. When the crystals are in this form, they are not piezoelectric. Below the Curie temperature the crystals exhibit tetragonal symmetry (Figure 2.3, right). Cubic crystal structure implies that the dimensions of all sides of the crystal are equal, whereas the tetragonal structure has one elongated side. This elongation allows the titanium (or zirconium) atom to “rattle” between the larger oxygen atoms. This has been shown below in figure 2.4.

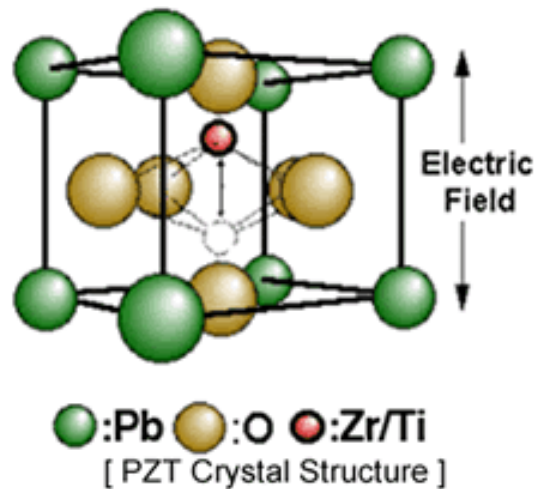


Fig. 2.4: A schematic of the PZT unit cell showing the “rattling” of the Zr (or Ti) atom

The “rattle” also allows charge separation between the positive and negative ions which causes an electric dipole behavior. Localized groups of dipoles with parallel orientation are called Weiss domains. However, the Weiss domains are randomly oriented in the PZT ceramic material. No piezoelectric properties are observed due to this randomness. To obtain piezoelectric behavior, an electric field in excess of 2000 V/mm is applied to the piezo-ceramics at an elevated temperature. The electric dipoles align and roughly stay in alignment upon cooling. Such a material shows piezoelectric behavior, and as a result, when an electric voltage is applied to a poled piezoelectric material, the Weiss domains increase their alignment proportional to the voltage. The result is a change in the dimensions (expansion, contraction) of the PZT material.

The importance of the Curie temperature can be further illustrated by the phase diagram of PbTiO_3 and PbZrO_3 , as shown in figure 2.5 below. Depending on the relative composition of Ti and Zr, the structure of PZT exhibits either a rhombohedral or tetragonal structure, and the Curie temperature is also affected. The phase boundary seen at $\text{Zr/Ti} \sim 0.52/0.48$ is known as the morphotropic phase boundary, and it has been shown that the piezoelectric properties are best at this composition. The target used for RF sputtering for this current project also has this same composition.

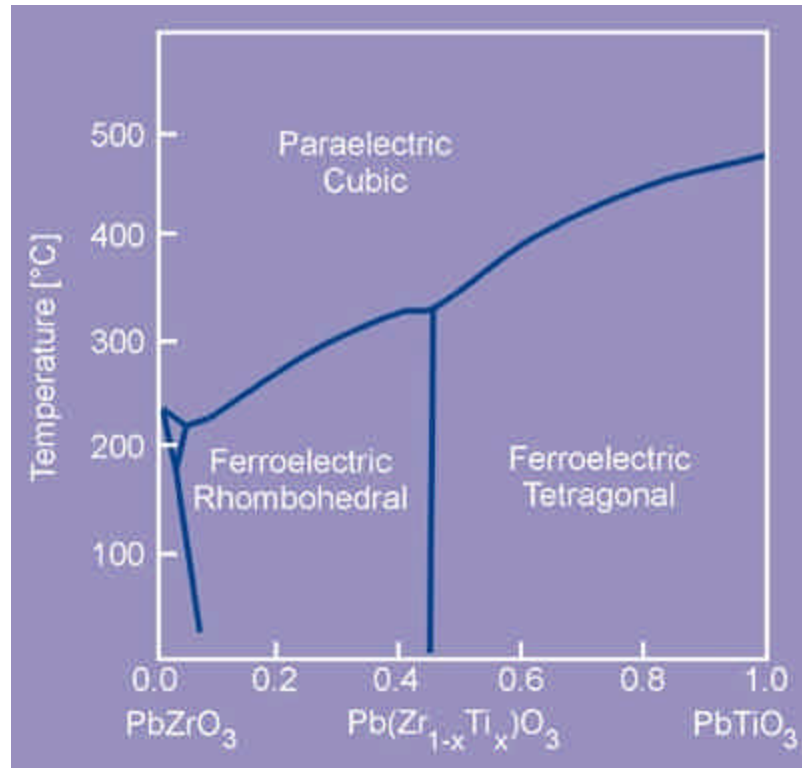


Fig. 2.5: The PbZrO_3 – PbTiO_3 phase diagram

Because a piezoelectric ceramic is anisotropic, physical constants relate to both the direction of the applied mechanical or electric force and the directions perpendicular to the applied force. Consequently, each constant generally has two subscripts that indicate the directions of the two related quantities, such as stress and strain for elasticity.

2.3.2 Fabrication Aspects

The two primary processes by which PZT is deposited in thin film form are:

Sol-gel deposition

A sol is a dispersion of the solid particles in a liquid where only the Brownian motions suspend the particles. A gel is a state where both liquid and solid are dispersed in each

other, which presents a solid network containing liquid components. The sol-gel coating process usually consists of the following steps:

1. The desired colloidal particles once dispersed in a liquid to form a sol.
2. The deposition of sol solution produces the coatings on the substrates by spraying, dipping or spinning. The latter is used as the preferred method for PZT-based sols.
3. The particles in sol are polymerized through the removal of the stabilizing components and produce a gel in a state of a continuous network.
4. The final heat treatments pyrolyze the remaining organic or inorganic components and form an amorphous coating. Annealing is then required to form the crystalline phase.

As can be seen from the steps above, the sol-gel method is a rather tedious method of obtaining films of PZT. Also, these steps need to be followed for multiple coatings to get the desired film thickness.

RF magnetron sputtering

In its simplest representation, the phenomenon of sputtering consists of material erosion from a target on an atomic scale, and the formation of a thin layer of the extracted material on a suitable substrate. The process is initiated in a glow discharge produced in a vacuum chamber under pressure-controlled gas flow. Target erosion occurs due to energetic particle bombardment by either reactive or non-reactive ions produced in the discharge.

This process is relatively simpler when compared to the sol-gel one. A single PZT target of the desired composition or multiple targets of PbZrO_3 and PbTiO_3 can be used. The one disadvantage of RF sputtering is that the control over the film composition is not as accurate as it is for sol-gel films. Taking these factors in to consideration, RF sputtering was chosen as the preferred technique for the current project.

A similar study as before has also been performed by Tamagawa *et al.* [3]. Here they have specifically studied PZT thin films on silicon only, and compared that with the information available in the literature on ZnO. They have presented an important conclusion: if the deposition parameters be optimized, then RF sputtering of the PZT films proves to be a better technique than the sol-gel process. This is because sputtering techniques are easier to incorporate into silicon micromachining methods. This is a must if these materials are to be used for MEMS devices. Sol-gel processes can be considered to be more “messy” as compared to the RF sputtered process, and requires a lot more effort and time.

Although RF sputtering may give higher values of the resistance at the resonant frequency, it should still be the preferred procedure for MEM resonators to be capable of incorporation into large scale industrial production. Therefore, the properties of the sputtered PZT films are of prime importance, and this is a direct consequence of the properties of the target that is used for sputtering.

Velu *et al.* [4] have tried different recipes for targets used for PZT RF sputtering. They maintained the molar ratio of (Zr/Ti) constant at (0.54/0.46), which is close to the tetragonal-rhombohedral morphotropic phase boundary described before. Near this boundary, PZT ceramics have high electro-mechanical coupling and low coercive fields [5]. They varied the molar concentration of PbO in the target mix between $X=1.0$, which is the stoichiometric composition, and $X=1.75$. The substrate temperature was also varied between $T_s=500^{\circ}\text{C}$ and $T_s=580^{\circ}\text{C}$. They found that the combination ($X=1.1$, $T_s=510^{\circ}\text{C}$) proved to be the optimum one. For all other proportions, either an oxygen deficient phase was present, or a lead deficient phase was present. The analysis by x-ray diffraction studies showed that for the (1.1, 510) combination, the single crystalline PZT perovskite (111) phase was present without any other unwanted phases. Due to the high substrate temperature, a post annealing process was not required. However, in a later article by the same group, Dogheche *et al.* [6] showed that a ($X=1.5$, $T_s=550^{\circ}\text{C}$) is a better mix composition, as it gives the highest value of the piezoelectric coefficient e_{31} at around -5.2 C/m^2 . In either case, the point put across by the authors was that heating the substrate is beneficial, because it results in in-situ crystallization of the perovskite PZT (111) phase, and this eliminates the need for post-annealing treatments.

Lee *et al.* [7] have shown that controlling the deposition temperature is of prime importance as it determines the orientation of the film, which in turn controls the electrical properties. They too concluded that the (111) orientation of the films gives good properties, like increased capacitance and increased remnant polarization. However, Lian *et al.* [8] and Taylor *et al.* [9] have shown that a (100) preferred orientation has a

higher piezoelectric coefficient, while in fact the (111) has the lowest. These films were prepared by the sol-gel method, and therefore it cannot be said for sure whether the same can be applied to RF sputtered films. Since we are more concerned with piezoelectric properties, depositing the (100) preferred orientation using sputtering needs to be examined.

Some of the unique properties of RF sputtered PZT thin films deposited on platinized silicon substrates are discussed below.

Haccart *et al.* [2] studied the effects of film thickness on the dielectric, ferroelectric and piezoelectric properties of sputtered PZT thin films. Their latter findings are very significant in defining some unique characteristics of PZT. It turns out that the d_{31} piezoelectric coefficient increases with thickness up to a saturation point, after which it stabilizes at that value. However, the d_{33} coefficient monotonically increases with the thickness of the film. This is not so in the case of ZnO, where these values are almost constants. The film thickness at which d_{31} starts stabilizing is about $0.6\mu\text{m}$, although other researchers like Lee *et al.* [10] have reported that this value is close to $1\mu\text{m}$. The value reported is about -38pm/V for the saturated d_{31} value, while the d_{33} increased from 45 to 80 pm/V for film thicknesses of $1\mu\text{m}$ and $1.7\mu\text{m}$ respectively.

The reason given for this unusual behavior of PZT is that a “dead” interfacial layer exists between the PZT film and the platinum electrodes, which reduces the effective thickness of the film. Also, as the film thickness increases, there is an increase in the ferroelectric

domain density and the domain wall mobility. These reasons have been stated as facts, and no substantial explanation has been given to support these.

This fact can however be used to our benefit. If we are to cause vibration in a mode which brings the d_{33} coefficient into play, then just by controlling the film thickness, the piezoelectric behavior of the resonator can be manipulated. An increase in the thickness will increase the d_{33} value, which in turn will reduce the effective resistance at resonance and increase the Q-factor or efficiency of the resonator. This will allow resonance at much higher frequencies as compared to the current ZnO devices.

There is, however, a limit to how thick the film can be. A very thick layer will inhibit the vibration and will accelerate damping, thus bringing down the Q-factor. Therefore, a balance of film thickness and damping must be assured to get high Q.

Lian *et al.* [8] have also reached a similar conclusion. They obtained increasing d_{33} values for increasing film thickness, and also found that the field induced strains and the weak field dielectric constants of the films increased with an increase in the film thickness. These films were produced by the sol-gel method and it can be inferred that this property of PZT thin films holds good without regard to the preparation technique. Taylor *et al.* [9] have studied rhombohedral PZT thin films, again produced by the sol-gel method, and concluded that d_{33} is controlled by a competition between the crystallographic orientation, film clamping by the substrate and by ferroelectric domain wall displacements.

2.4 PZT versus ZnO – COMPARISON OF PROPERTIES

Tjhen *et al.* [1] studied the properties of ZnO and PZT thin films on silicon substrates for micromechanical devices and systems. The ZnO was deposited using RF sputtering and the PZT using the sol-gel method. They studied mainly the mechanical and the piezoelectric properties of these films. The results they obtained, as well as data collected from other sources, give us a good comparison of the two materials. This is presented below in Table 2.1 below and explained thereafter.

Table 2.1: Comparison chart of electro-mechanical properties of PZT and ZnO

Property	PZT thin films	ZnO thin films
Piezoelectric coefficient (d_{33})	45 – 80 pC/N [2] (RF sputtered)	10.5 – 11.5 pC/N (RF sputtered)
	190-250 pC/N (sol-gel produced)	
Young's modulus	1 to 5 ($\cdot 10^{10}$) N/m ²	15 to 24 ($\cdot 10^{10}$) N/m ²
Electromechanical coupling factor	0.2 (sputtered) 0.3-0.6 (sol-gel produced)	0.08 (sputtered)
Dielectric constant	800 – 1100	10.8 – 11
Electrical resistivity	$0.02 \cdot 10^7 - 1 \cdot 10^7$ ohm-m	$0.25 \cdot 10^7 - 1 \cdot 10^7$ ohm-m
Crystal structure	Perovskite [11]	Hexagonal wurtzite [11]

The primary comparison is to be made based on the resistance that can be attributed to the piezoelectric film in the device. The total impedance consists of the inductance, capacitance and the resistance part. These three components can be written as:

$$L_{m,n} = \frac{M_n}{h^2} \quad C_{m,n} = \left[\frac{K_n}{h^2} \right]^{-1} \quad R_{m,n} = \frac{nph\sqrt{Er}}{Qd_{31}^2 E_p^2 w}$$

At resonance, the value of the inductance and the capacitance is the same. Therefore, the only impedance to motion is the resistance, R . This has to be reduced in order to achieve higher efficiency. The factors which can be controlled are the quality factor (Q), the value of $(d_{31}^2 E_p^2)$, which corresponds to the properties of the piezoelectric material, and of course the width of the resonator, w . Therefore, if by changing the piezoelectric material we can get a higher value of $(d_{31}^2 E_p^2)$, then that should be preferred. Going by this assumption, if we were to find a range for the value of $(d_{31}^2 E_p^2)$ based on the table above, we would get 24800 – 76000 for ZnO, and 36100 – 1562500 for PZT. When RF sputtered PZT thin films are considered, the value comes out to be between 2025 and 160000. Therefore, the deposition procedure must ensure that the properties of the films should be comparable to the higher values of the piezoelectric coefficient and the Young's modulus as reported in the literature.

Another important parameter is the electromechanical coupling factor, or k . It can be defined as the ratio of the amount of output mechanical energy to the total energy present in the resonator. From the table, it is clear that PZT has a much higher k value, and this

maybe attributed to the difference in crystal structure. More information on the crystal structures of both PZT and ZnO can be found at the website of the Materials Science and Engineering Division, Naval Research Laboratories, Washington D.C. [11].

As a final conclusion, exploring PZT as a substitute to ZnO will definitely prove beneficial in enhancing the frequency response and the quality factors of the resonators.

CHAPTER 3

IMPLEMENTATION

3.1 DESIGN AND MODELING OF PIEZOELECTRIC RESONATORS

There were two primary shapes of these resonators which were examined.

- Clamped-clamped beam resonators

These were examined as preliminary simple devices for low frequency operation by Gianluca Piazza [28] as part of the same project. These resonators operated in their out-of-plane bulk extensional modes. An analogous real world example of these resonators can be a guitar string, which also resonates in several higher order harmonic modes similar to these devices. A schematic of a beam resonator was shown previously in figure 1.2, and has been shown here again in figure 3.1 and 3.2.

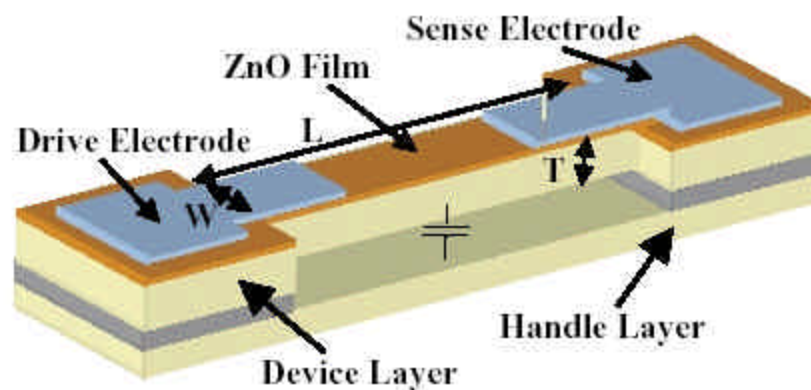


Fig. 3.1: A schematic of a piezoelectric clamped-clamped beam resonator

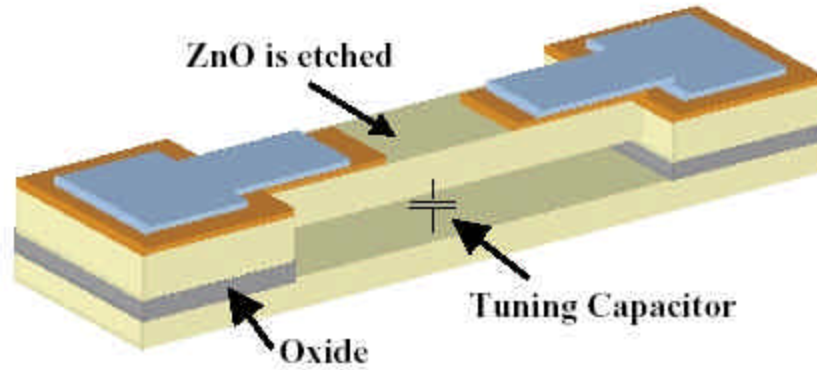


Fig. 3.2: A schematic of a beam resonator showing tuning capability

As can be seen from the above diagram that due to the inherent fabrication technique employed using silicon-on-insulator (SOI) substrates, a tuning capacitor was also formed between the device layer silicon and the handle layer silicon. This gave control over the resonance frequency and it could be adjusted by applying a DC voltage and varying this capacitance.

ANSYS simulations of the mode shapes of a beam resonator are shown in figure 3.3.

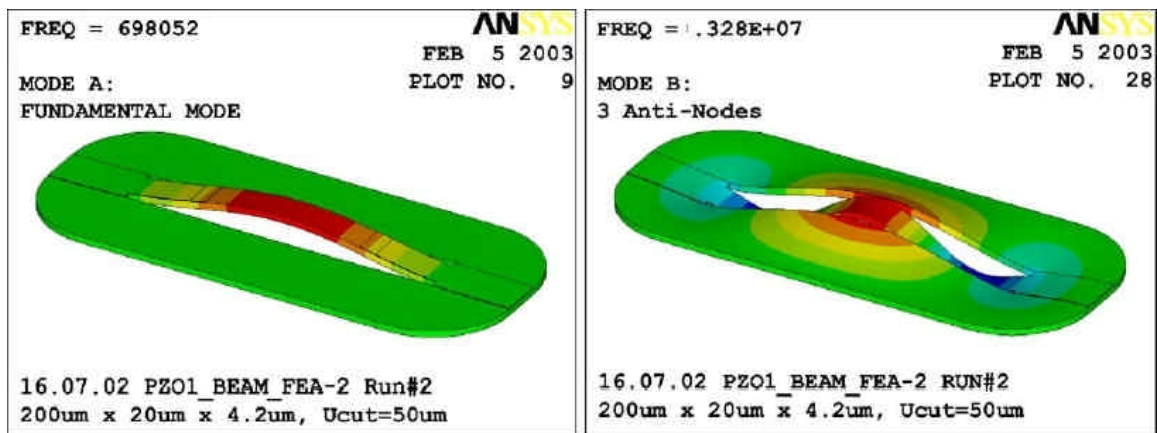


Fig. 3.3: The fundamental (L) and third order (R) mode shapes for a 200 μ m beam

- Length-extensional two-port block resonators

The motional impedance of beam resonators is high, and therefore cannot be applicable for high-frequency operation beyond 5-7MHz. Two-port block resonators were therefore examined for the purpose of enhancing the operating frequencies of these resonators. A schematic of a block resonator with ZnO as the piezoelectric material is shown below in figure 3.4.

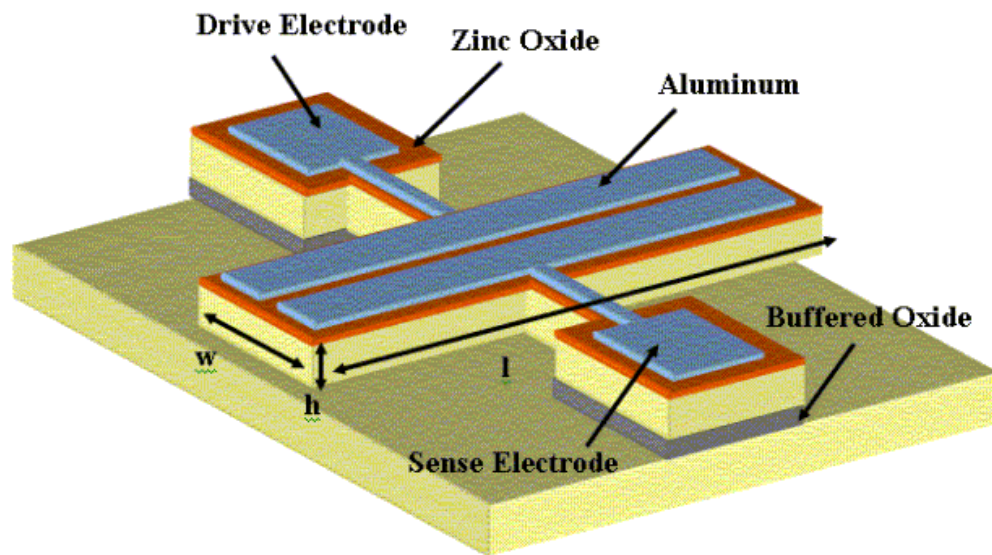


Figure 3.4: A schematic of a two-port length extensional piezoelectric block resonator

Accurate modeling of these block resonators requires the understanding of the equivalent electrical circuit representation. This has been shown below in figure 3.5.

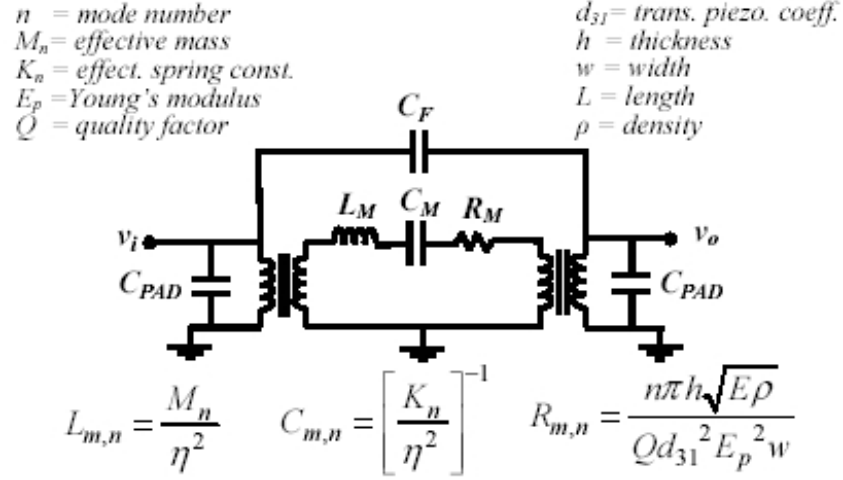


Fig. 3.5: The equivalent electrical circuit representation of a two-port block resonator

It can be seen from figure 3.5 that the input and output ends have been modeled as two transformers, with the primary resonator body being represented as a series LCR circuit. The contact pads on either end are for wire bonding the devices during testing. Since both ZnO and PZT are dielectric materials, there is a capacitance C_{PAD} that is present on either end.

The two salient features of the above circuit are the LCR resonator body and the feed-through capacitance C_F going from the input to the output. As mentioned before in section 2.4, L and C of the resonator cancel each other out at resonance, leaving only the motional impedance, R_M , to be concerned with. This needs to be minimized, which in turn correlates to the reduction of the $(d_{31}^2 E_p^2)$ factor. The other component of concern is the feed-through capacitance. This can more basically be described as the “noise” that transfers from the input to the output. It is a challenge to reduce this feed-through level to a minimum for piezoelectric resonators, because the device starts resonating as soon as

alternating current is applied, or in other words, as soon as it is connected to the network analyzer for testing. In the case of capacitive resonators, unless a drive voltage is applied, there is no transduction, giving the convenience of removing this feed-through before operating the device using proper calibration techniques.

One way of reducing the feed-through is having a low resistivity ground plane for these devices. In the schematic shown above, the device layer silicon (resistivity = 0.05 $\Omega\cdot\text{cm}$) is used as the ground plane. It would be favorable if a metal ground plane were incorporated. This would reduce the feed-through level as now the electric field which forms across the piezoelectric layer will be completely confined between the top metal electrode and ground metal layer, giving better transduction of the signal from input to output and reducing loss. Characterization and implementation of a metal ground plane has been discussed later in this chapter.

ANSYS simulations of the mode shapes are shown below in figure 3.6.

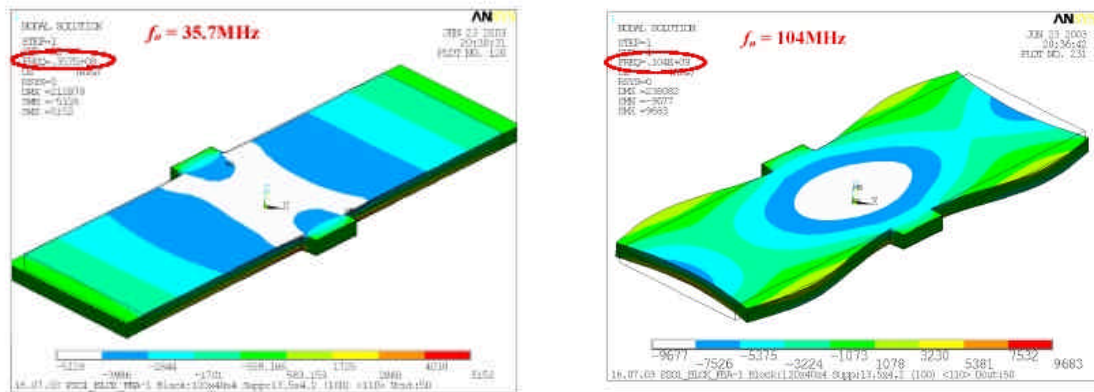


Fig. 3.6: First (L) and third (R) extensional modes for a 120 μm by 40 μm block resonator

3.2 FABRICATION AND CHARACTERIZATION OF ZNO-BASED BLOCK RESONATORS

3.2.1 RF Sputtering of ZnO

RF sputtering has been established as the easiest and most reliable method of obtaining single crystalline ZnO films on silicon. The parameters for RF sputtering on heated substrates have been characterized thoroughly, and are given below in table 3.1.

Table 3.1: RF sputtering parameters for ZnO

<u>Parameter</u>	<u>Value</u>
Power	135W
Gases used	Argon and Oxygen
Flow rates	25sccm Ar + 25sccm O ₂
Sputtering pressure	6mTorr
Substrate temperature	210°C
Time	4000 seconds
Film thickness on silicon	~0.35μm

X-ray diffraction (XRD) analyses of the sputtered ZnO films confirm their crystalline behavior with a preferred (002) orientation. It is imperative that the piezoelectric material be single-crystalline or exhibit preferential orientation otherwise its properties will be severely affected. The XRD plots have been shown below in figure 3.7.

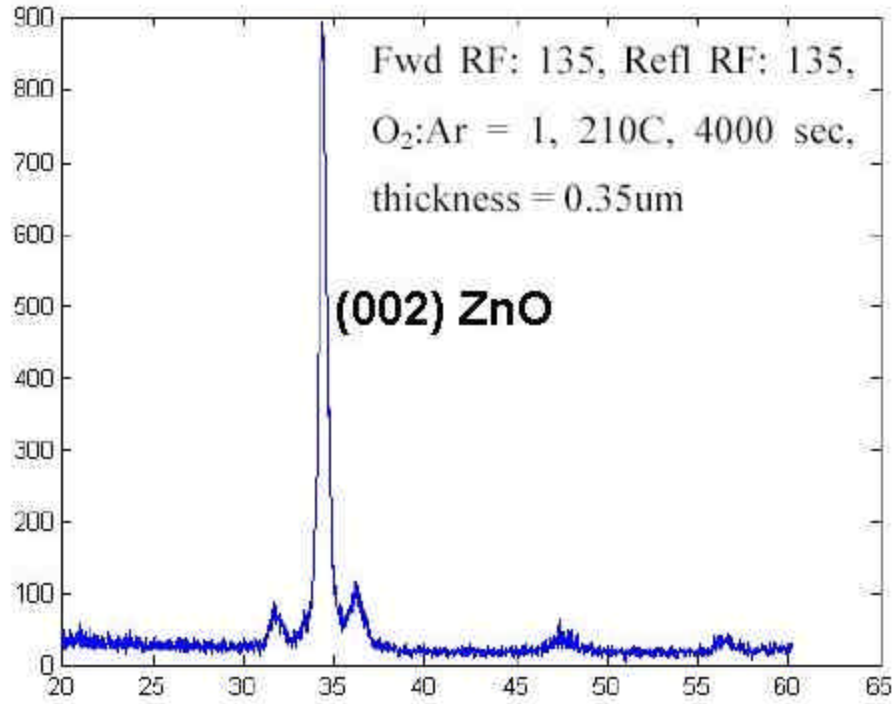


Fig. 3.7: XRD plot for RF sputtered ZnO showing (002) preferred orientation

3.2.2 Implementation of an additional etch mask

Before explaining the need for an additional photolithography mask, it is instructive to elaborate on the process flow for fabrication that was being followed previously. This has been illustrated below in figure 3.8, and then each step has been described in detail later on with schematics of the masks used at each step.

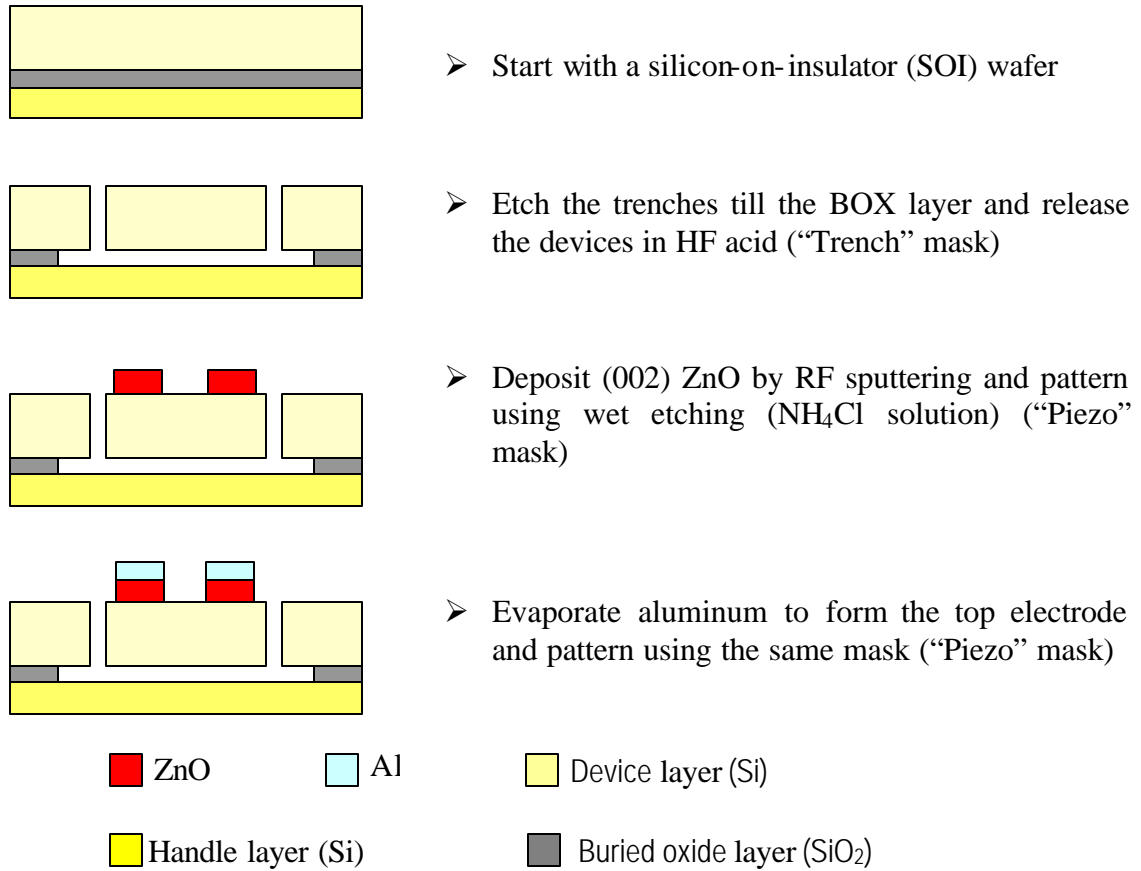


Figure 3.8: Process flow for fabrication of ZnO-based MEM resonators

A silicon-on-insulator (SOI) wafer is taken with a $5\mu\text{m}$ device layer and a $2\mu\text{m}$ buried oxide (BOX) layer. The following steps are performed on it:

1. Trenches are etched using the STS ICP after patterning photoresist SC1813 using the “Trench” mask. The resist is then stripped and ashed to give a clean wafer. A schematic of this mask is given below in figure 3.9.

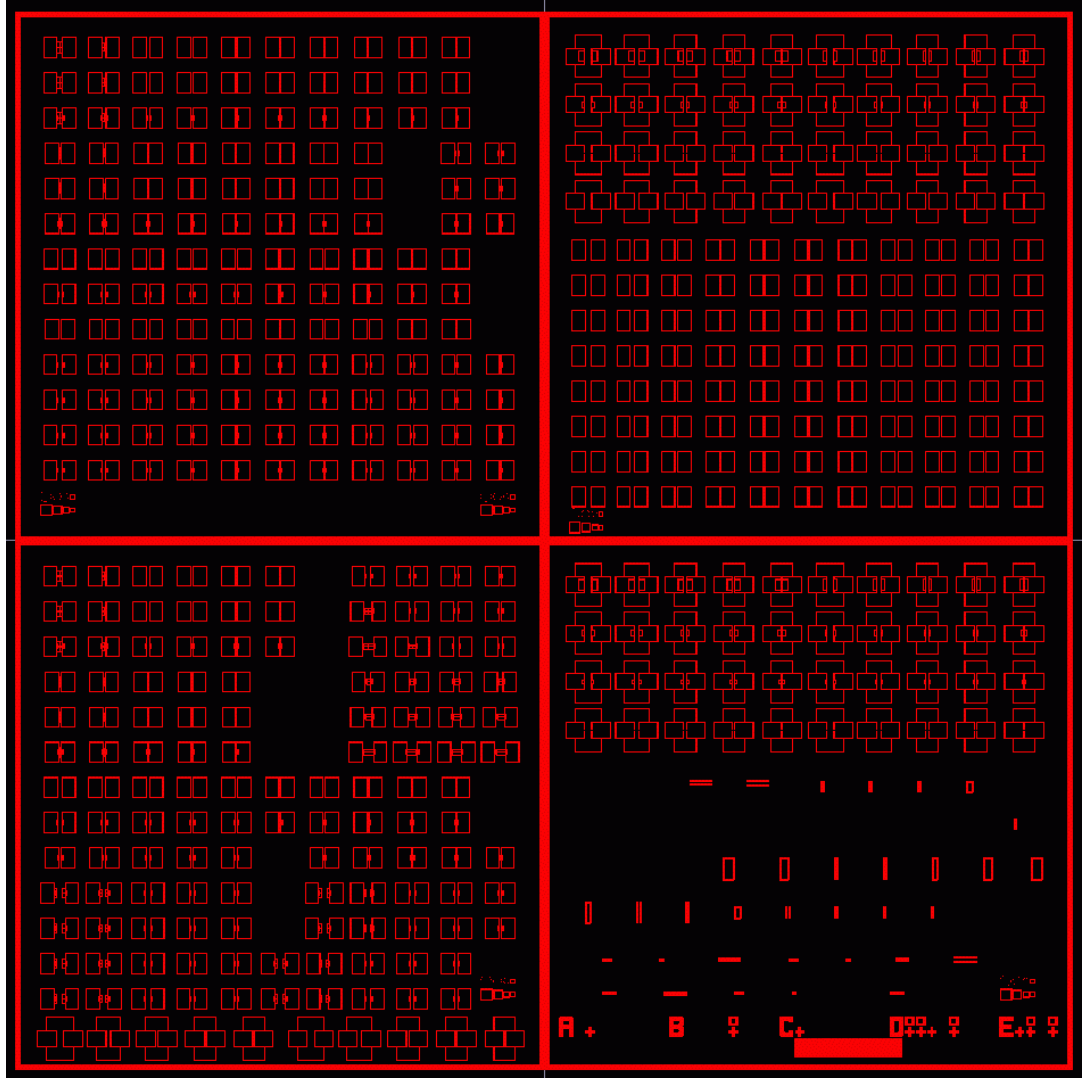


Fig. 3.9: A schematic of the “Trench” mask used for patterning the resonator body

2. Release of the devices is then done in 49%HF + DI water (1:1), whereby the buried SiO_2 layer was etched off through access points provided by the trenches. The release is done until the $40\mu\text{m}$ characterization mark comes off. The wafer is then kept in HF for another 5 minutes, giving approximately $25\mu\text{m}$ undercut on either side. The devices targeted on this wafer are the smallest five out of the ten present, namely the

10, 20, 25, 30 and 40 μ m wide devices. A 40 μ m wide released block resonator is given below in figure 3.10. Unless all of the buried oxide is completely etched away by the HF, the device will not be a free-standing resonator, and therefore cannot oscillate. A 60 μ m wide device which has not been released completely is also given below in figure 3.11. Figure 3.12 shows a released 30 μ m block resonator with the 25 μ m undercut on either side.

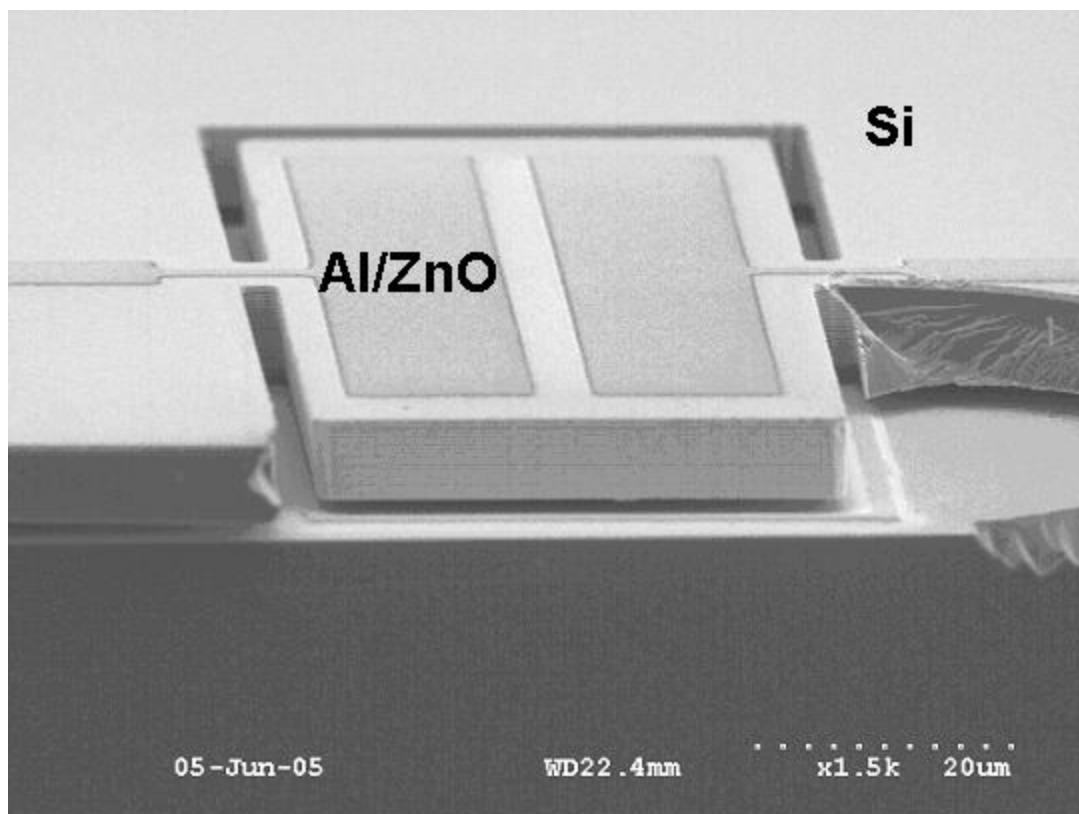


Figure 3.10: An SEM picture of a completely released 40 μ m block resonator

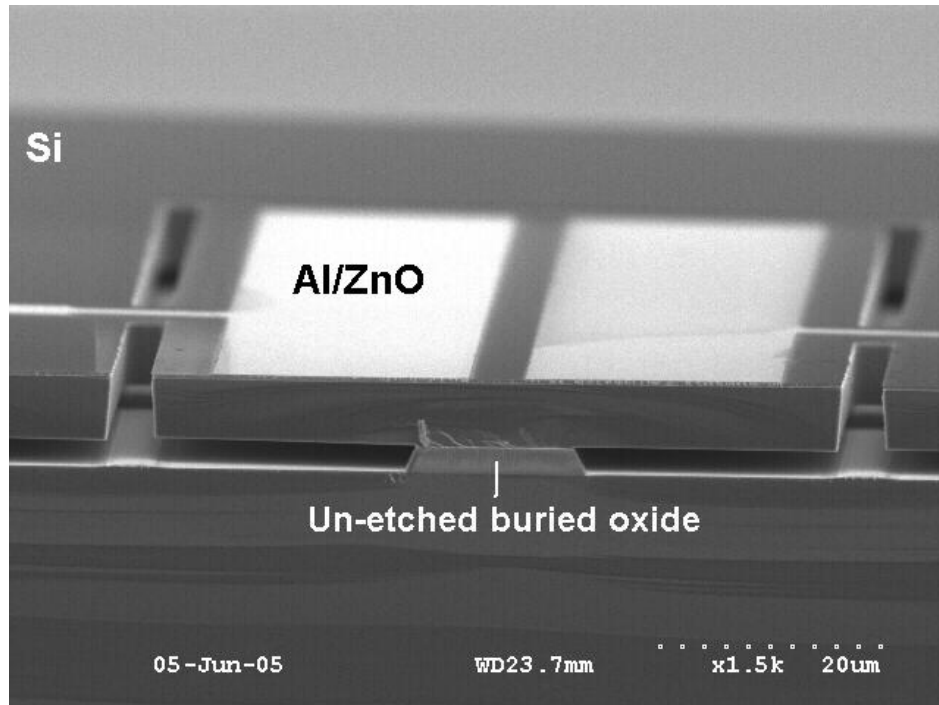


Fig. 3.11: An SEM picture of a partially released 60 μ m wide block resonator. This device is not free to resonate and therefore is non-functional.

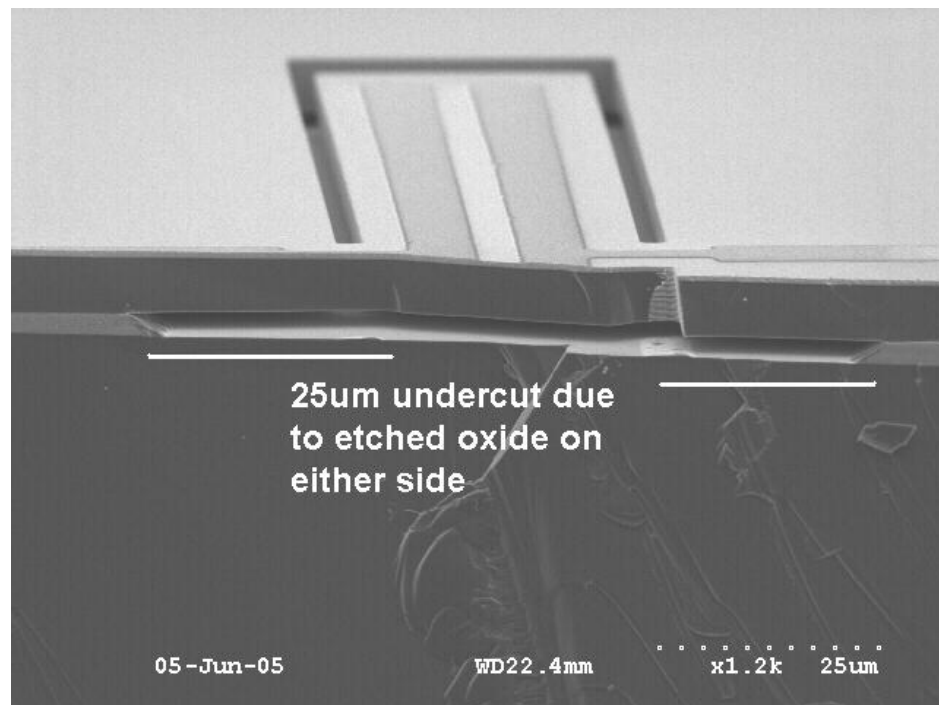


Fig. 3.12: An SEM picture of a released 30 μ m block resonator showing oxide undercut

3. Approximately $0.35\mu\text{m}$ of ZnO is then RF sputtered on the device layer silicon.
4. The next step is patterning the ZnO layer. Resist SC 1813 is patterned on this using the “Piezo” mask. A schematic of this mask is given below in figure 3.13.



Fig. 3.13: A schematic of the “Piezo” mask used for patterning the piezoelectric layer and the top electrode

Good alignment between this layer and the trench layer is absolutely essential. The parameters for the exposure time using ultraviolet radiation in the mask aligner and

development time using MF-319 developer solution for the resist were characterized prior to any processing on the SOI. The optimum parameters are given below in table 3.2.

Table 3.2: Positive resist SC 1813 parameters

<u>Parameter</u>	<u>Value</u>
Spin parameters	3000rpm, 30s.
Bake parameters	100°C, 60s.
Exposure parameters	21 mW/cm ² , 7.5 secs.
Developing parameters	MF-319, 4.5 minutes
Hard bake parameters	120°C, 10 minutes

5. A 5% NH₄Cl solution is then prepared for wet etching of ZnO. This is heated to 60°C, and the SOI wafer is immersed in this solution while it is being stirred. Etching of 0.35µm ZnO takes about 6-7 minutes. The wafer is observed under microscope at regular intervals to ensure a proper etch.
6. The resist is then stripped in 1112-A stripper by dipping the wafer in it for 6-8 minutes.
7. The next step is to evaporate aluminum and pattern it using the same mask. This *double patterning for the ZnO and the top electrode* has to be done because Al cannot be used as an etch mask for the underlying ZnO. The etchant for ZnO attacks Al also.

The steps followed for this are as follows:

- 1000Å of Al is evaporated using the e-beam evaporator on patterned ZnO.
- Resist SC1813 is patterned using the same “Piezo” mask.
- The etchant for aluminum is a solution mix of $\text{K}_3\text{Fe}(\text{CN})_6$ (1gm) + KOH pellets (1gm) + 100ml DI water. This is a good wet etchant and does not attack the underlying ZnO.
- The wafer is then immersed in the above-mentioned etchant. Etching 1000Å of Al takes about 90 seconds.

It can be visualized from the above process flow and from figure 3.8 that if there is even a slight misalignment between the top aluminum layer and the ZnO layer, then the aluminum will get shorted to the device layer silicon. This will cause failure of the device as now there will be no electric field across the piezoelectric layer. The alternating current will flow from the top electrode to the ground plane and not through the ZnO layer.

To eliminate this possible cause of shorting of these devices, it was thought that an additional etch pits mask be incorporated into the process flow. Simply put, these etch pits are “holes” in the ZnO layer for access to the ground plane, but since they are separated from the primary device body, any misalignment will not short the device. A schematic of this mask, when implemented on a wafer, is given below is figure 3.14.

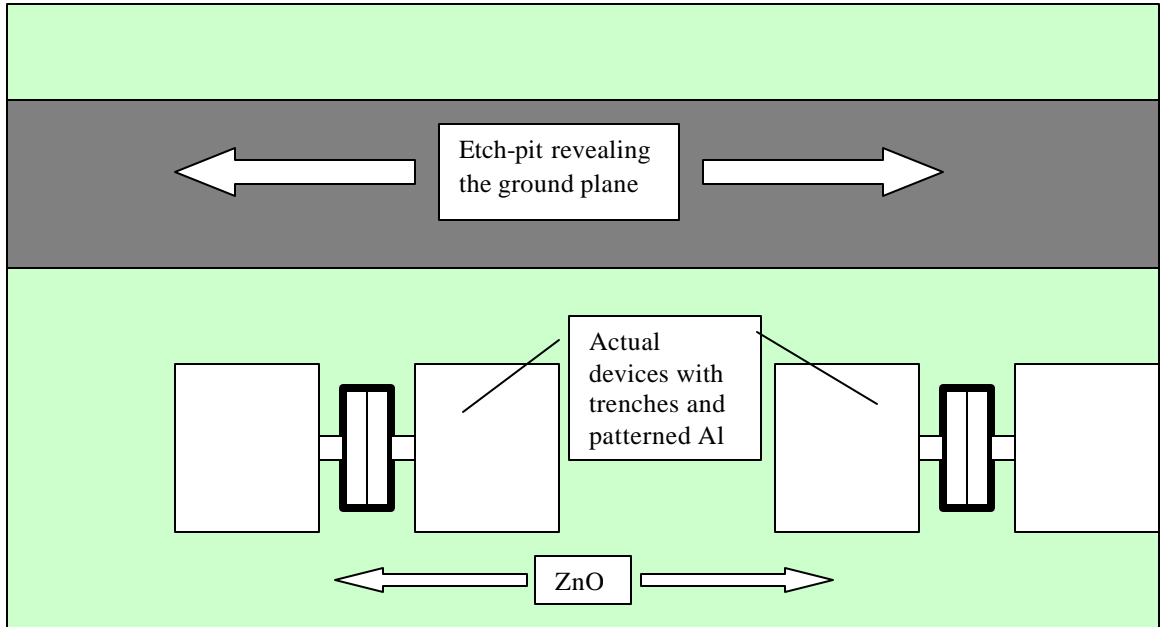


Fig. 3.14: Schematic of the new configuration for ZnO resonators with an additional mask for etch-pits. Because the ZnO over the actual devices is not being patterned, the possibility of shorting the top and ground planes is avoided.

A test run was performed on a dummy wafer before incorporating this mask on to the SOI. Given below are some optical microscope pictures revealing the etch pits before and after ZnO etching (figures 3.15 and 3.16).

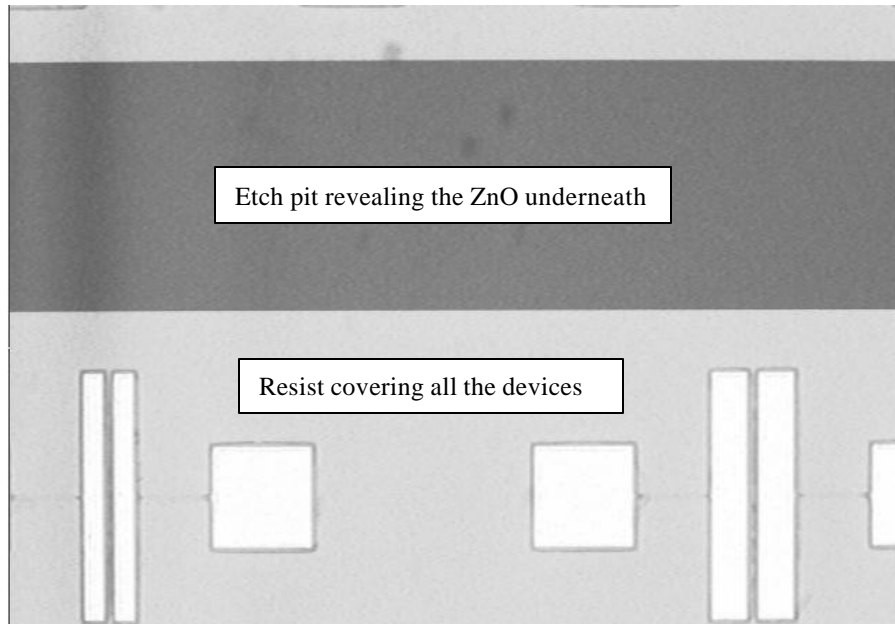


Fig. 3.15: Implementation of the additional etch-pits mask: prior to ZnO etching

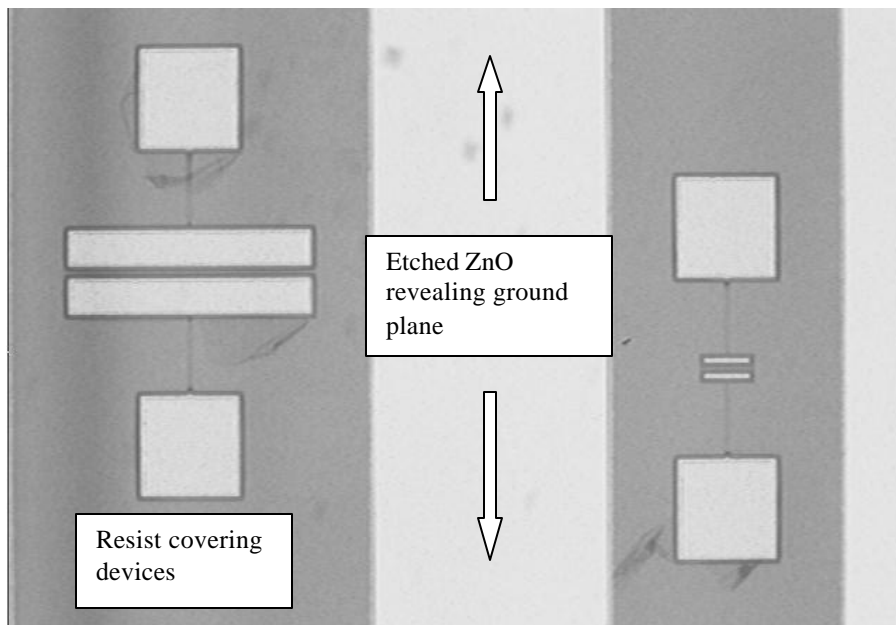


Fig. 3.16: Implementation of the additional etch pits mask: after ZnO etching

3.2.3 Implementation of a metal ground plane

As discussed in section 3.1, it is important to have a low resistivity ground plane for piezoelectric MEM resonators in order to reduce the feed-through level and obtain higher transduction from input to output.

A chrome metal ground plane was tried out, as it has been shown to act as a good adhesion layer as well as seed layer. However, chrome does not serve its purpose well.

1. The resistivity of the ground plane did not reduce by a large factor. It was about 1-2 kilo-ohms before, and it reduced to about 220 ohms with chrome. There was some unknown error during fabrication which caused the resistivity to be that high.
2. ZnO does not grow as well on chrome when compared to single-crystalline silicon. This was proved by the fact that small variations in the gas flow rates during RF sputtering of ZnO on chrome gave rise to polycrystalline films. This is shown below in figure 3.17.

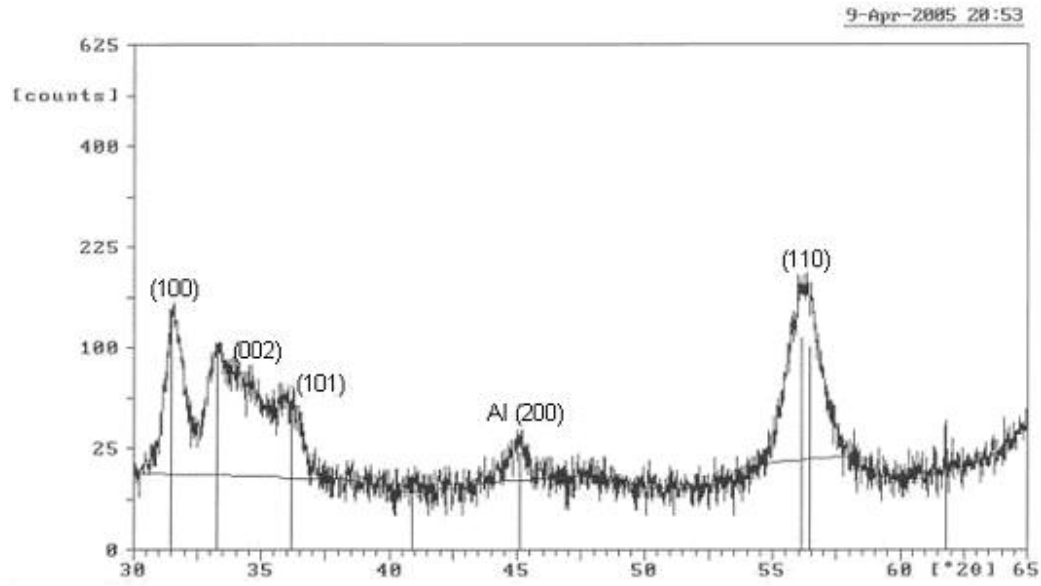


Fig. 3.17: XRD pattern of ZnO showing a polycrystalline film

This caused the ZnO film to have poor dielectric properties, and on application of alternating current, the film broke down and would short the top and ground chrome electrodes.

The other option for the ground plane was the metal gold [27]. 2000Å of gold were deposited on a bare silicon test wafer with a 200Å chrome adhesion layer. Approximately 0.5µm of ZnO was grown on this gold film via RF sputtering at 210°C. Usually, deposition for 4000 seconds gives ~0.35µm of ZnO on silicon or on chrome. However, on gold, the deposition rate seems to be higher, and 0.5µm was obtained. This was proved by SEM pictures, as given below in figures 3.18 and 3.19.

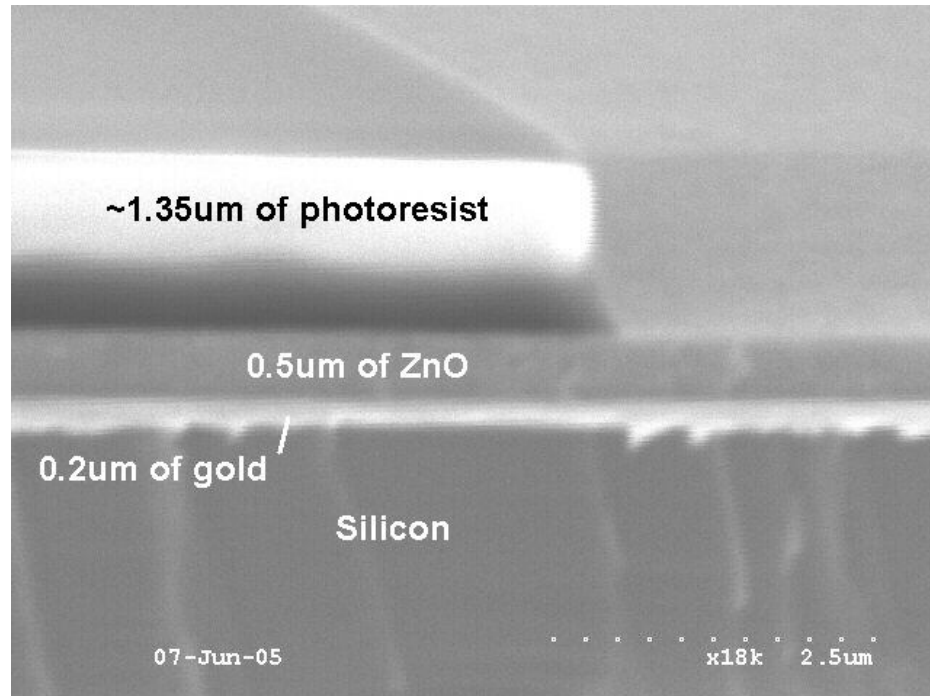


Fig. 3.18: SEM picture showing the use of a gold ground plane for ZnO sputtering: the different layers prior to ZnO etching

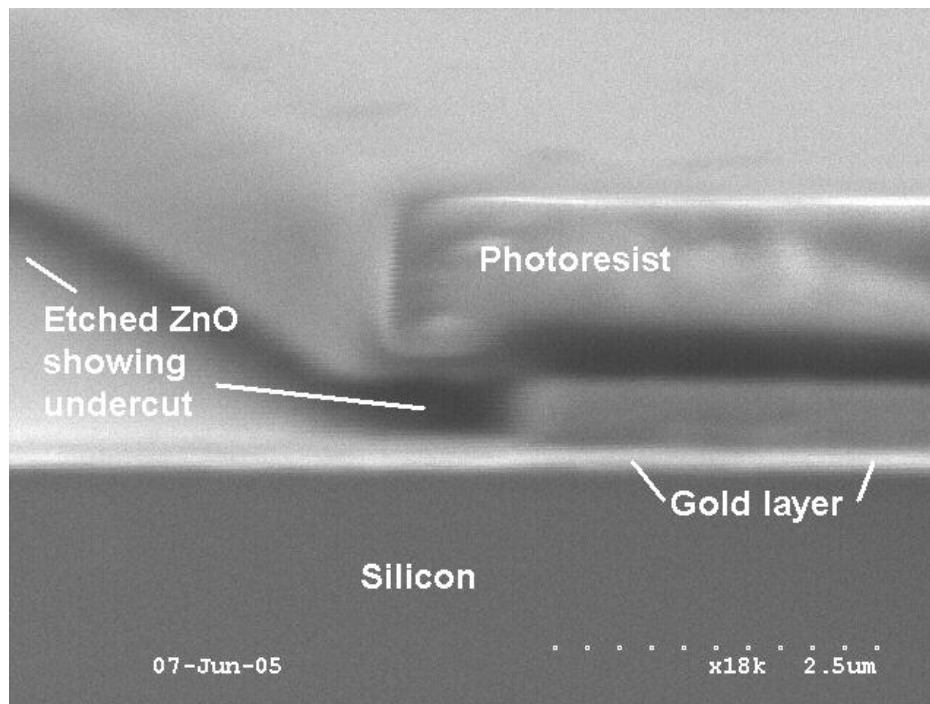


Fig. 3.19: SEM picture showing the use of a gold ground plane for ZnO sputtering: after ZnO etching in 5% NH_4Cl solution.

The XRD plot of ZnO on Au is given below in figure 3.20.

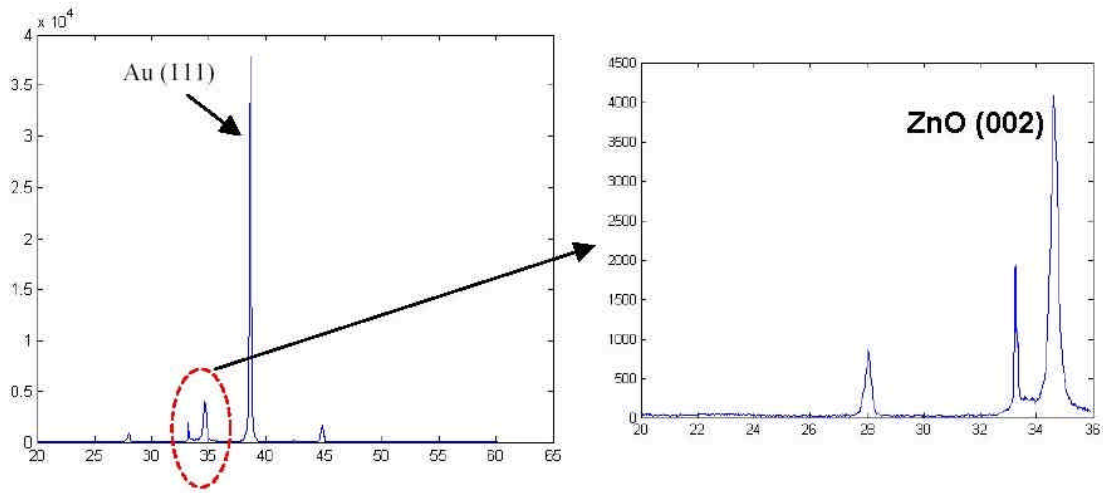


Fig. 3.20: XRD plot of ZnO on Au/Si showing a preferred (002) growth

Even though the (002) peak in the above figure is not very high, it is still showing a preferred orientation. The biggest advantage of using gold is that the ground plane resistivity is about 1 ohm, which will ensure the reduction in the feed-through level significantly. Gold is therefore, the chosen candidate for the ground plane for ZnO devices.

3.2.4 Final process flow

After the implementation of the additional etch-pit mask and the gold ground plane, the revised and more efficient process flow for ZnO-based MEM resonators is given below in figure 3.21.

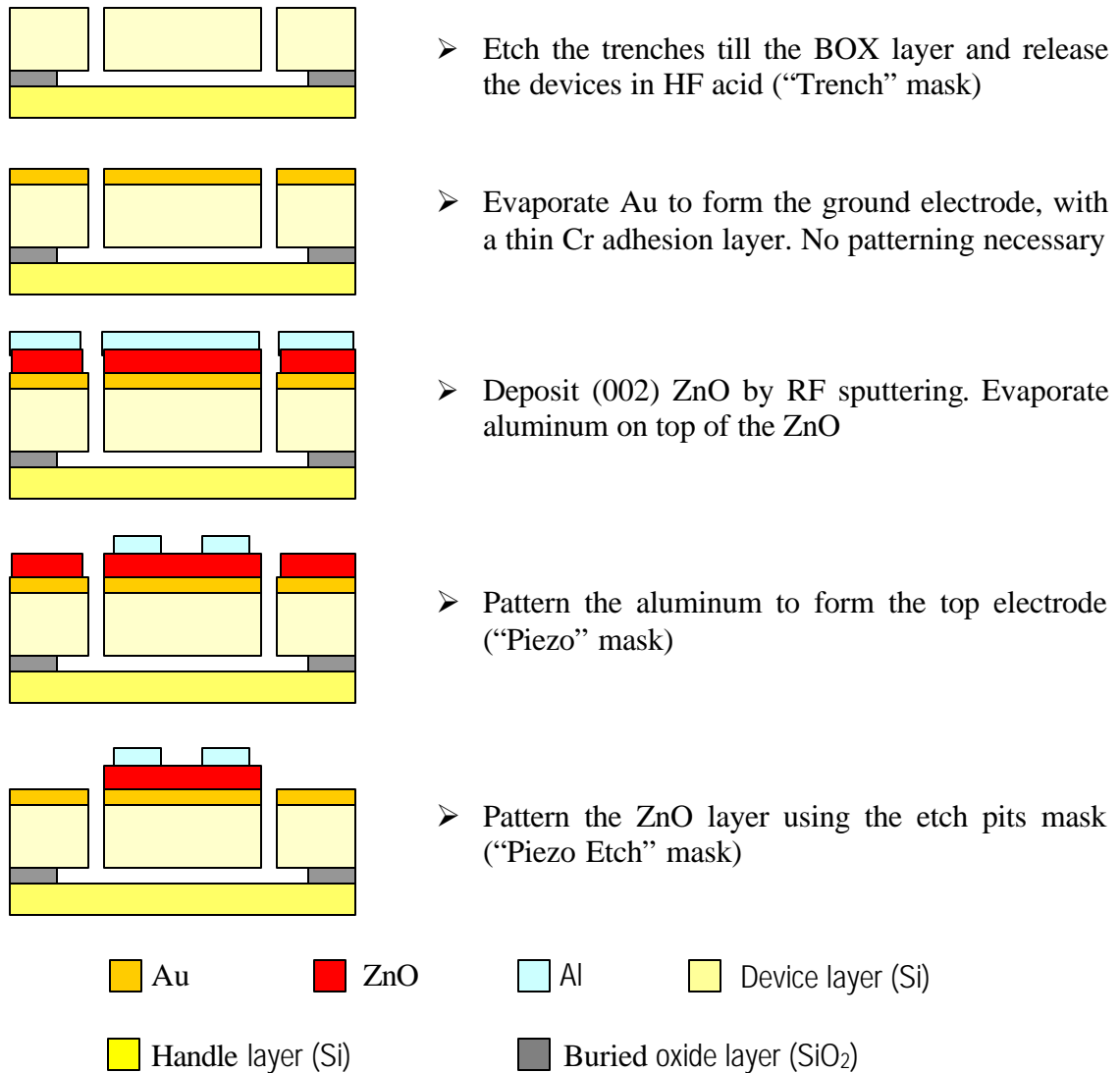


Figure 3.21: Revised process flow for fabrication of ZnO-based MEM resonators

Some SEM pictures of devices fabricated with this process flow are given below in figures 3.22 through 3.24.

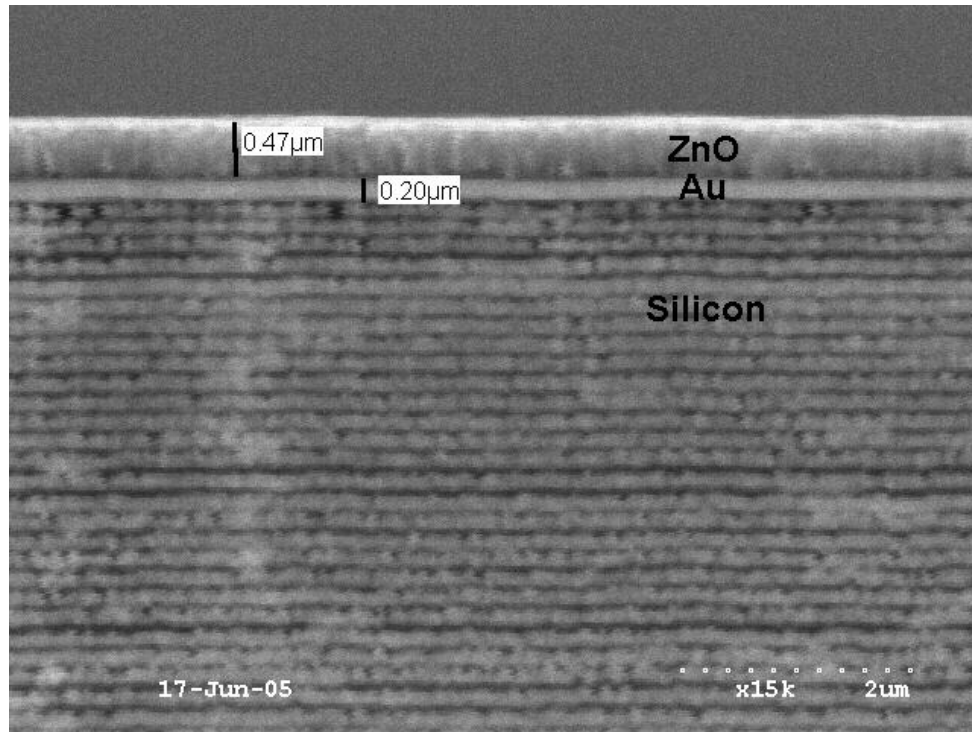


Fig. 3.22: The cross-section of a major trench in the SOI showing the different layers

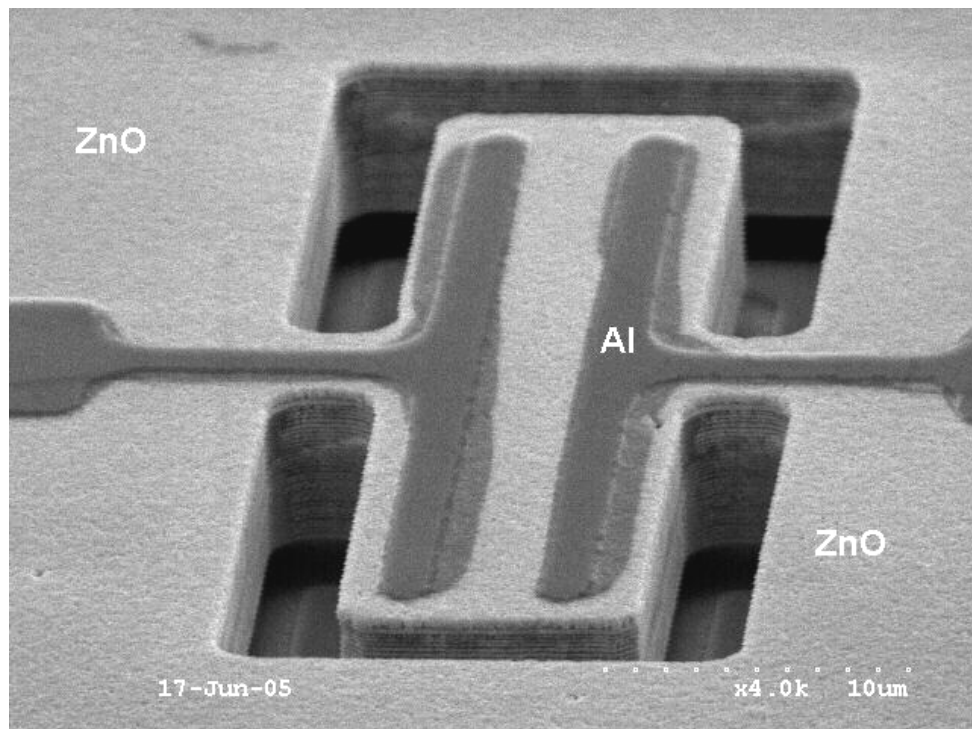


Fig. 3.23: A 40µm by 10µm block resonator. This is the smallest possible working device on the current batch.

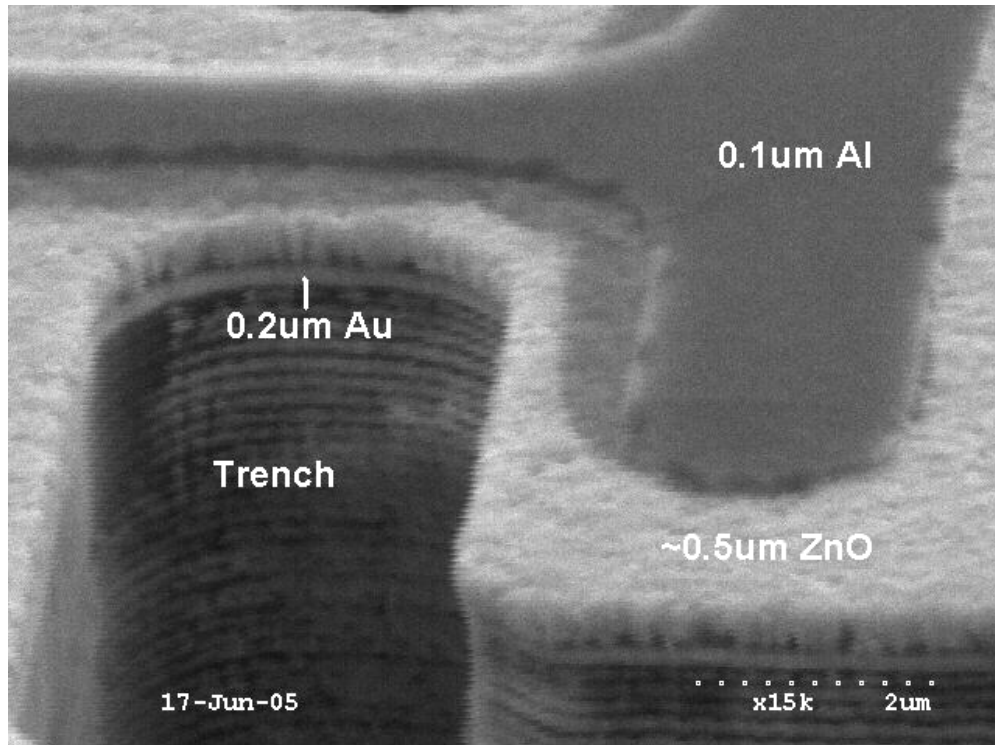


Fig. 3.24: This figure shows the close-up details from a 20 μm by 10 μm block resonator. This is the smallest device on the current mask-set, but the traces could not be patterned properly because of the limitations of the mask aligner in the clean room.

3.3 FABRICATION AND CHARACTERIZATION OF PZT-BASED BLOCK RESONATORS

3.3.1 RF Sputtering of PZT

RF sputtering was chosen as the preferred technique for PZT also for reasons described previously in section 2.3. There were many variations to the sputtering recipe which were examined. Unlike the sputtering of ZnO where the substrate was heated to obtain a crystalline film, PZT sputtering was carried out at room temperature. This was done because of there was no facility for heating of the substrate on the PZT sputtering station. The films were annealed using a rapid thermal processing (RTP) unit to obtain crystalline films. This provides more control over the properties of the thin film.

Two PZT targets were purchased from Ferroperm-Piezo Ceramics (Denmark) for this purpose. There had been some modifications in the RF sputterer in the clean room since when the targets were ordered, and only 3" diameter targets were acceptable. The targets purchased were about 2.56" (or 65mm) in diameter. To correct this, a clamp for the target of the appropriate dimensions was manufactured in the Georgia Tech Research Institute (GTRI) machine shop. An older gun was also installed on to one of the stations (station 4), and this station will soon be dedicated for PZT sputtering only.

On reviewing the MSDS for PZT, it was found that in processes where powders are generated, for example sputtering, the powders can be considered as being pure lead. PZT as a compound contains about 50-70% Pb. Therefore, the clean room staff was wary about lead contamination in the sputterer. They were more bothered by the poisonous

nature of Pb than its presence having any effect on contamination of other samples inside the sputterer. After about six weeks of researching on this topic and taking help from experts, a solution was thought of. It was proposed that separate sputterer parts or “shields” be fabricated for the PZT process only. As a result, every time the PZT process is run, the user needs to change the parts inside the sputterer which will be in contact with the sputtered PZT. These parts included three plates which would cover the other targets, and one cylindrical part which has to be substituted for the existing one. They too were fabricated in the GTRI machine shop.

One of the targets was tried out in the RF sputterer. The deposition process was working out fine, and the test runs were being carried out on a glass substrate. The entire run, which was for about thirty minutes, was not completed just to check whether deposition was taking place or not. On opening the chamber, it was found that the target had cracked, although some deposition had occurred. The power level used was 125W, which is about 3.8 W/cm^2 . In the literature the power levels go up to 140-150W for efficient sputtering [2], but the target in question here cracked at a power level less than that. The reason for this is that in the literature, most RF sputtering was done using multiple targets of Pb, TiO_2 and ZrO_2 , or PbTiO_3 and PbZrO_3 , while we have used a single target of PZT. The single target is more brittle when compared to the individual targets, and so the power supply must be kept as low as possible. A thorough understanding of the different sputtering parameters that can be altered taking into consideration the limitations of the clean room here at Georgia Tech is warranted at this stage.

Sputtering power

The higher the power level is, the thicker the film will be. It was thought to increase the power gradually from 50W (minimum allowed in the sputterer) in intervals of 10W and observe the film in order to get the best possible quality and thickness without causing damage to the target. At 50W, the film of PZT is so thin (less than 10nm) that it cannot be properly differentiated using the SEM. No considerable change in the thickness was observed at 55W or 60W also. When sputtering was carried out at 70W, then a reasonably thick PZT layer was observed with a thickness of about 80nm after post-annealing. Power was then increased to 80W and no damage was observed to the target after sputtering for 3 hours. It must be noted here that all sputtering is carried out on silicon wafers with a layer of platinum evaporated on to it. Platinum requires a titanium adhesion layer also, as it does not stick to silicon that well. The power is therefore set at 80W, as there is a good chance that the target might crack on increasing it any further. A cross-sectional SEM picture of as-sputtered PZT/Pt/Ti on silicon is given below in figure 3.25, showing approximately 50nm of PZT. The 3.5” mentioned on the figure is the substrate-target distance, which will be explained later.

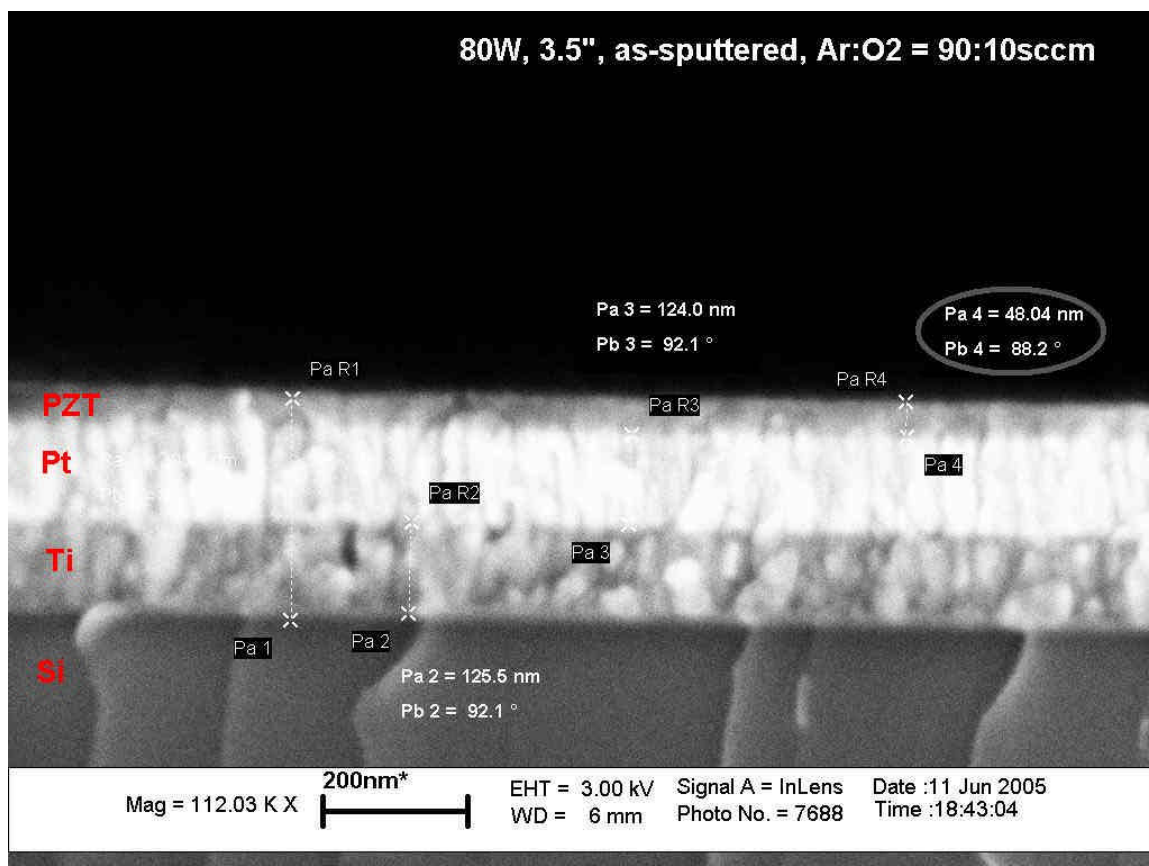


Fig. 3.25: SEM cross-section showing as-sputtered PZT/Pt/Ti/Si at 80W

Sputtering time

This is set at about 2.5 to 3 hours. It has been reported that the sputtering time cannot be indefinitely increased to get a thicker film. If sputtering is done for longer times, then the oxygen content in the film reduces, giving rise to the undesirable pyrochlore phase of PZT. This deteriorates the piezoelectric properties of the film.

Substrate-target distance

Generally, the smaller the distance, the thicker the film will be. However, the disadvantage of this is that the film quality of the film degrades as this distance is reduced. Previously, this distance was set at about 3.5", which is close to 90mm. The target distance was adjusted by the staff later on, and it was increased to 5" (~130mm). A SEM cross-section of the as-sputtered film with the distance set at 5" is given below in figure 3.26.

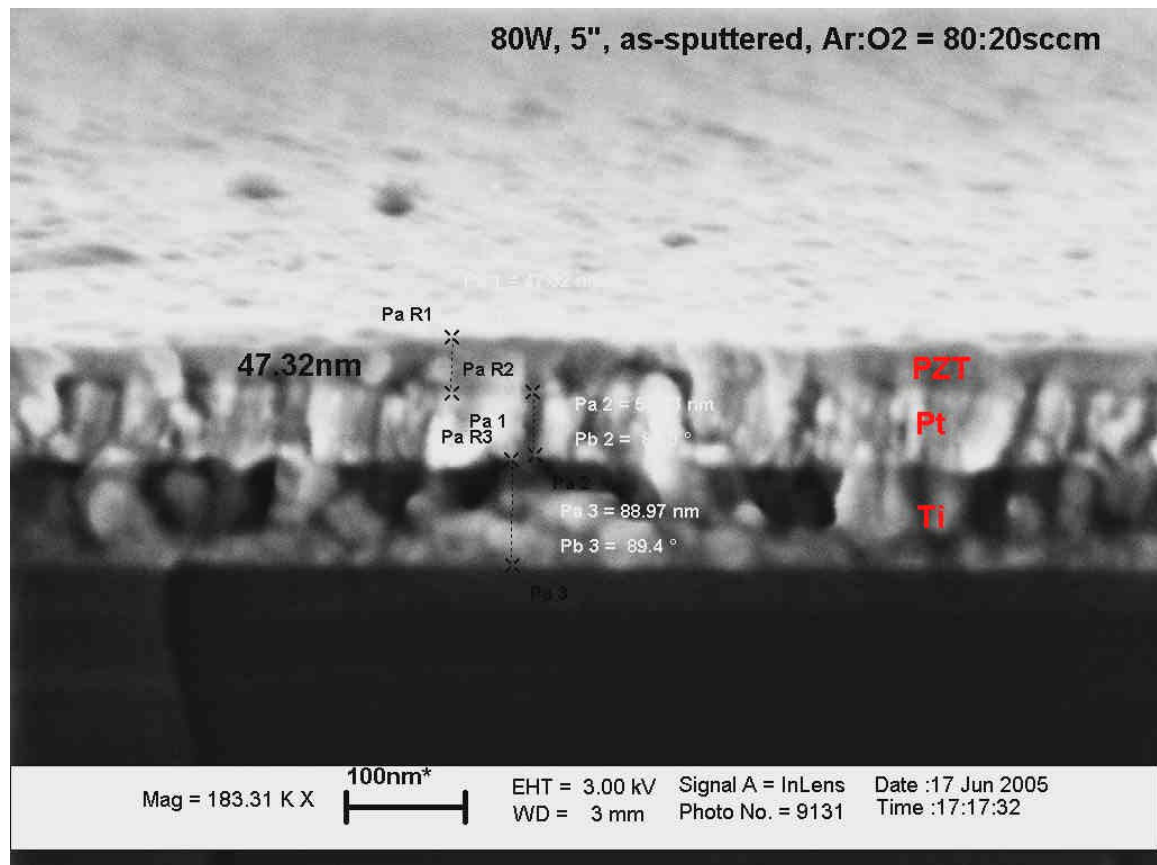


Fig. 3.26: SEM cross-section showing as-sputtered PZT/Pt/Ti/Si with a 5" substrate-target distance

It has been reported that good quality PZT films have been obtained using a substrate-target distance of 60mm, which corresponds to about 2.5" [26]. Sputtering was carried out under these conditions, and the SEM cross-sectional view is given below in figure 3.27.

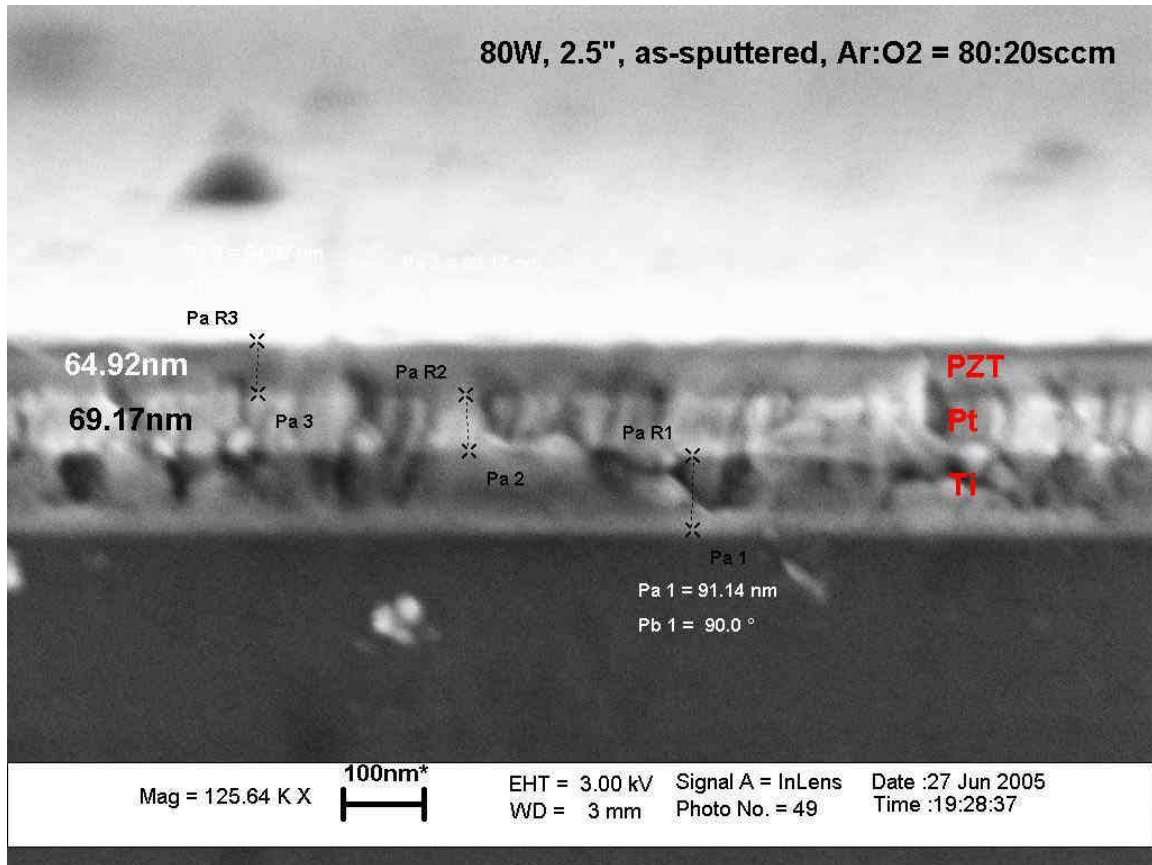


Fig. 3.27: SEM cross-section showing as-sputtered PZT/Pt/Ti/Si with a 2.5" substrate-target distance

Shown below in figure 3.28 is the variation of the thickness of the as-sputtered film as a function of the substrate-target distance.

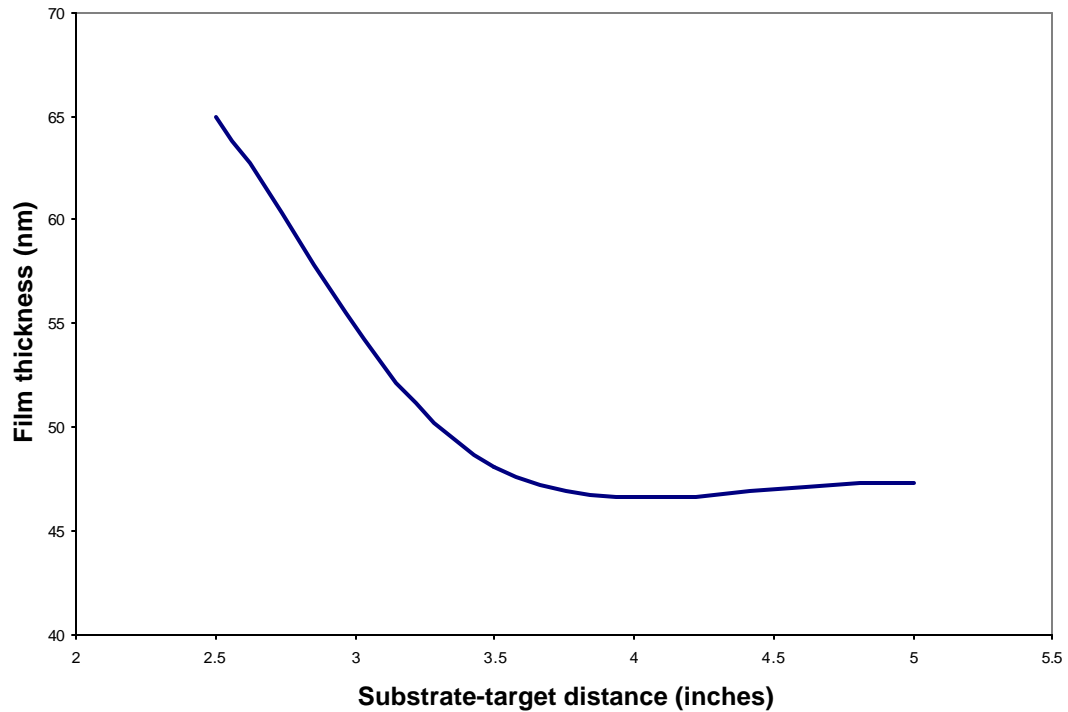


Fig. 3.28: The as-sputtered PZT film thickness as a function of the substrate-target distance

It can be noted that the varying the distance beyond 4" does not have much effect on the film thickness, but as the distance gets smaller (less than 3"), the thickness increases more rapidly.

The effect on the quality of the film has been discussed with respect to PZT crystallinity in section 3.3.2 below.

Gas flow rates/sputtering pressure

Increasing the sputtering pressure usually gives thicker films and also improves the quality of the film by reducing micro-cracks and brittleness. The optimum sputtering pressure reported is about 8Pa (which corresponds to 60mTorr). The mass-flow

controllers installed on the RF sputterer here at Georgia Tech allow only to a maximum of 15mTorr, or 2Pa (98sccm argon and 10sccm oxygen). Therefore, this parameter cannot be modified any further, unless a higher order mass-flow controller is installed. The pressure is therefore fixed at 15mTorr for all the sputtering runs.

3.3.2 PZT crystallinity

As mentioned before, the RF sputtering of PZT thin films is carried out at room temperature and is then post-annealed in the rapid thermal processing (RTP) unit to obtain crystalline films. A number of recipes were tried out in the RTP to get the optimum set of parameters.

There are three parameters which can be varied during annealing:

Temperature and duration of anneal

PZT perovskite phase starts crystallizing at temperatures of 600°C and higher. Therefore, a number of recipes as obtained from the literature [2, 17, 26] were tried out and XRD plots were taken.

Even though the RF sputtering process and the post-annealing process are done separately, the PZT crystallinity is dependent on some of the sputtering parameters, such as the power and the target-substrate distance. However, the thickness of the PZT thin film is immaterial when it comes to determining the orientation.

Depending on the temperature, the duration was also fixed. Annealing for very long periods of time is detrimental to the quality of the film. The different combinations tried out are given below in table 3.3

Table 3.3: Rapid Thermal Annealing parameters for RF sputtered PZT thin films

<u>Recipe #</u>	<u>Temperature (°C)</u>	<u>Time (minutes)</u>
1	625	30
2	650	15
3	700	5
4	750	0.5

Hereafter, recipe 1 will be referred to as (625, 30), recipe 2 as (650, 15), recipe 3 as (700, 5) and recipe 4 as (750, 0.5).

Annealing atmosphere

Usually, all annealing is done in air or in a nitrogen atmosphere. Annealing in a pure oxygen atmosphere is not recommended, as much higher annealing temperatures will be required (>800°C). For the purpose of this work, a nitrogen atmosphere has been used.

The XRD plot for a sample with annealing done using (625, 30) on Ti/Si is given below in figure 3.29.

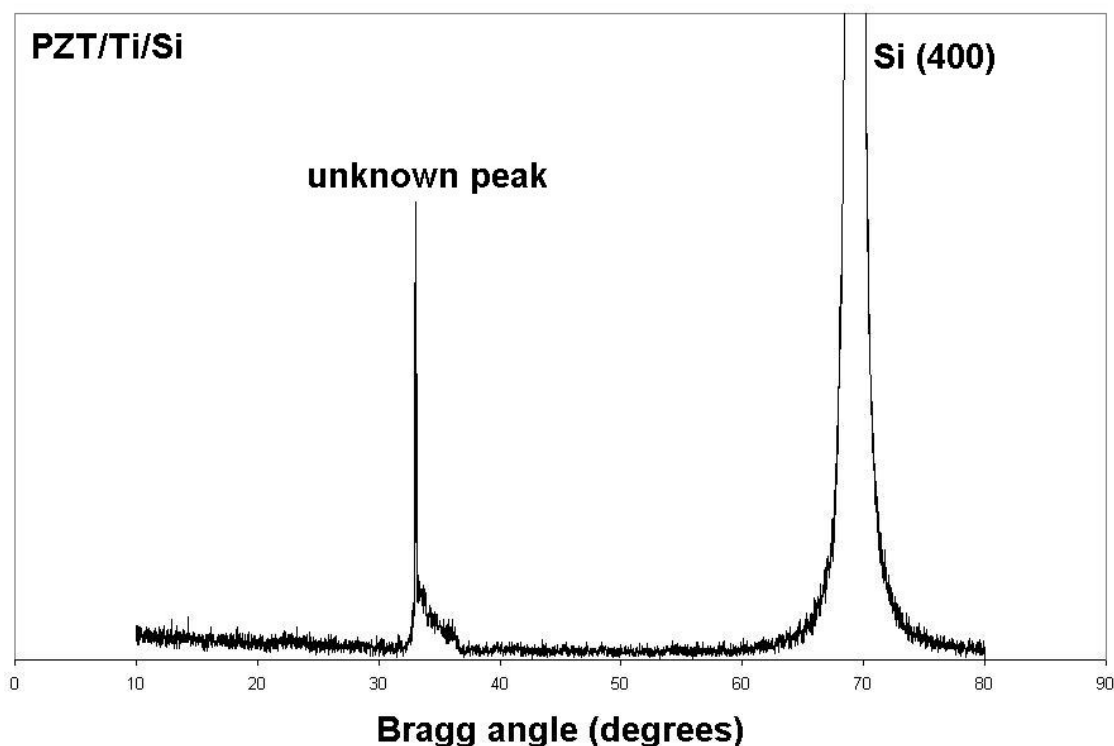


Fig. 3.29: XRD plot for PZT/Ti/Si with RTP done using (625, 30). The substrate-target distance is 3.5" and the power is 50W.

It must be noted that this PZT was deposited on Ti/Si and not on Pt/Ti/Si. This was done to verify the annealing recipe, and it was then thought that it could be extended onto Pt/Ti substrates also. However, the crystallinity of PZT is dependent on the substrate on which it grows, and further analysis showed that annealing on Ti/Si does not give the same results as annealing on Pt/Ti/Si. In fact, on Ti/Si, no peaks for PZT were observed. Instead, an unknown peak was observed at about 33° which was later believed to be coming from an interfacial compound (Si-O, Ti-Si-O). This peak has been filtered out in the XRD plots which follow. Since platinum is required as the ground plane for making PZT-based resonators, it is more relevant to study the crystallinity of PZT on Pt/Ti.

The following table summarizes the characterization of PZT crystallinity by varying sputtering parameters as well as the post-annealing recipe.

Table 3.4: Array of parameters varied for PZT RF sputtering and RTP annealing (80W, RTP done in pure N₂ atmosphere)

Sample #	Time (hours)	Distance between target and substrate (inches)	Temperature/time of anneal (°C/minutes)
1	2.5	3.5	As-sputtered
2	2.5	3.5	650/15
3	2.5	3.5	700/5
4	2.5	3.5	750/0.5
5	3	5	As-sputtered
6	3	5	650/15
7	3	5	700/5
8	3	5	750/0.5
9	3	2.5	750/0.5

XRD plots are provided for samples 2, 3, 4, 6, 7 and 8 below in figures 3.31 through 3.36 with relevant explanations given alongside. It is instructive to mention here that the preferred orientation is the (110) peak, the (111) peak or the (200) peak. The figure 3.30 below is a screenshot from the JCPDS database of the Bragg angles for Pb(Zr_{0.52}Ti_{0.48})O₃. The (101), (110) and the (200) peak have been highlighted.

33-0784						Wavelength= 1.54184					
<u>Pb(Zr_{0.52}Ti_{0.48})O₃</u>						2 θ	Int	h	k	l	
Lead Zirconium Titanium Oxide						21.432	9	0	0	1	
						22.024	12	1	0	0	
						<u>30.942</u>	<u>u</u>	<u>1</u>	<u>0</u>	<u>1</u>	
						<u>31.388</u>	<u>100u</u>	<u>1</u>	<u>1</u>	<u>0</u>	
						<u>38.284</u>	<u>15</u>	<u>1</u>	<u>1</u>	<u>1</u>	
Rad. CuK α λ 1.5418 Filter Ni Beta d-sp Diff						43.664	9	0	0	2	
Cut off Int. Diffract. 1/leor						44.918	16	2	0	0	
Ref. Kakegawa, K. et al., Solid State Commun., 24, 769 (1977)						49.426	5	1	0	2	
						50.418	6	2	0	1	
						50.418	6	2	1	0	
						53.392	5				
Sys. Tetragonal S.G.						54.736	12	1	1	2	
a: 4.036 b: c: 4.146 A: C: 1.0273						55.526	24	2	1	1	
α β γ Z: 1 mp:						64.436	9	0	2	2	
Ref. Ibid.						65.400	5	2	2	0	
						67.812	2	0	0	3	
						69.004	<u>u</u>	<u>2</u>	<u>1</u>	<u>2</u>	
						69.647	<u>6u</u>	<u>2</u>	<u>2</u>	<u>1</u>	
						69.647	6	3	0	0	
						72.227	6	1	0	3	
						74.067	9	3	0	1	
						74.067	9	3	1	0	
						76.590	2	1	1	3	
						78.381	2	3	1	1	
						85.102	<u>u</u>	<u>2</u>	<u>0</u>	<u>3</u>	
						86.038	<u>4u</u>	<u>3</u>	<u>0</u>	<u>2</u>	
						86.995	<u>u</u>	<u>3</u>	<u>2</u>	<u>0</u>	
						88.988	<u>15u</u>	<u>1</u>	<u>2</u>	<u>3</u>	
						90.026	<u>u</u>	<u>3</u>	<u>1</u>	<u>2</u>	
						91.092	<u>15u</u>	<u>3</u>	<u>2</u>	<u>1</u>	
						96.095	<1u	0	0	4	
						99.631	<1u	4	0	0	
						100.322	<1u	1	0	4	
						101.884	<1u	2	2	3	
						102.995	1	3	2	2	
						104.606	2	1	1	4	
						106.169	2	3	0	3	
						107.985	<u>u</u>	<u>4</u>	<u>1</u>	<u>1</u>	
						108.317	<u>4u</u>	<u>3</u>	<u>3</u>	<u>0</u>	
						110.599	1	1	3	3	
						112.477	1	3	3	1	
						113.450	2	2	0	4	
						116.416	<u>u</u>	<u>4</u>	<u>0</u>	<u>2</u>	
						117.240	<u>6u</u>	<u>4</u>	<u>2</u>	<u>0</u>	
						118.081	<u>u</u>	<u>1</u>	<u>2</u>	<u>4</u>	
						121.173	<u>1u</u>	<u>4</u>	<u>1</u>	<u>2</u>	

Fig. 3.30: The JCPDS XRD data showing the different Bragg angles for Pb(Zr_{0.52}Ti_{0.48})O₃. The underlined angles are 30.942 for (101), 31.388 for (110), 38.284 for (111) and 44.918 for (200).

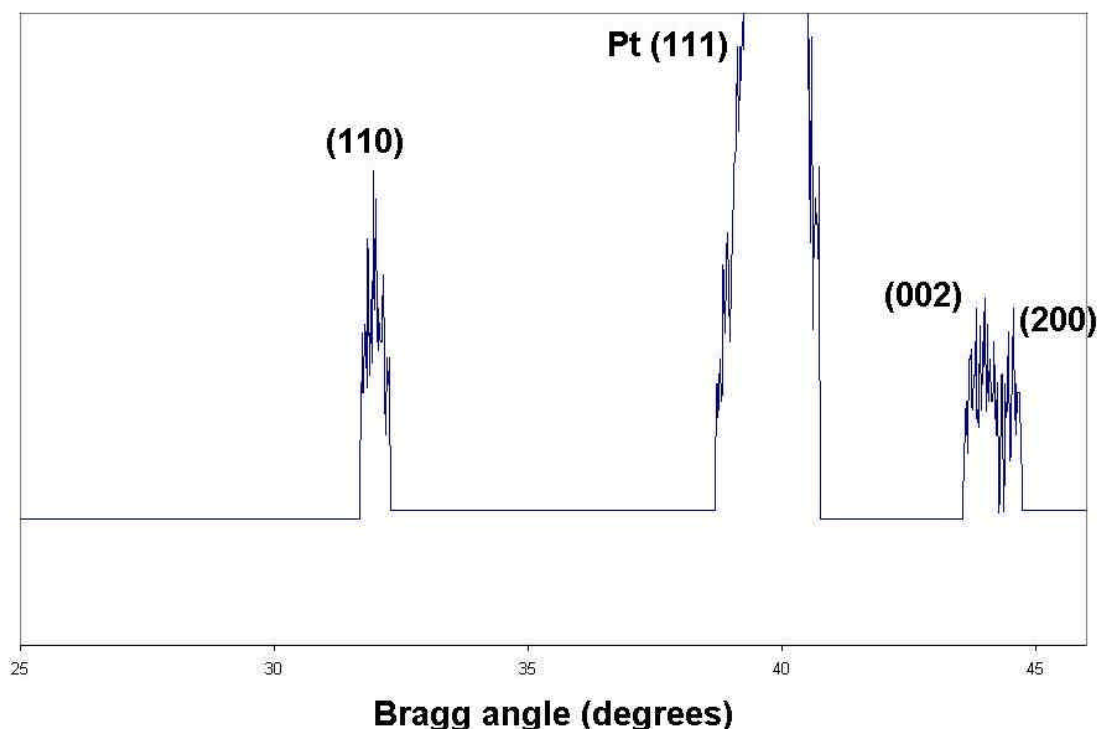


Fig. 3.31: XRD plot for PZT/Ti/Si with RTP done using (650, 15) for a substrate-target distance of 3.5". Unnecessary peaks/noise has been filtered out from the raw data.

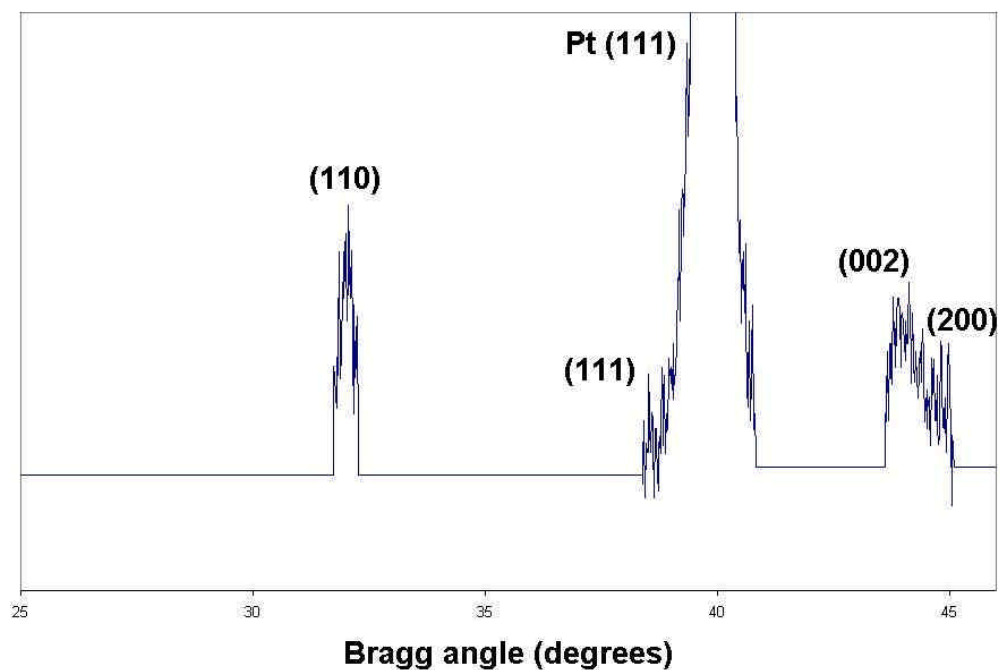


Fig. 3.32: XRD plot for PZT/Ti/Si with RTP done using (700, 5) for a substrate-target distance of 3.5".

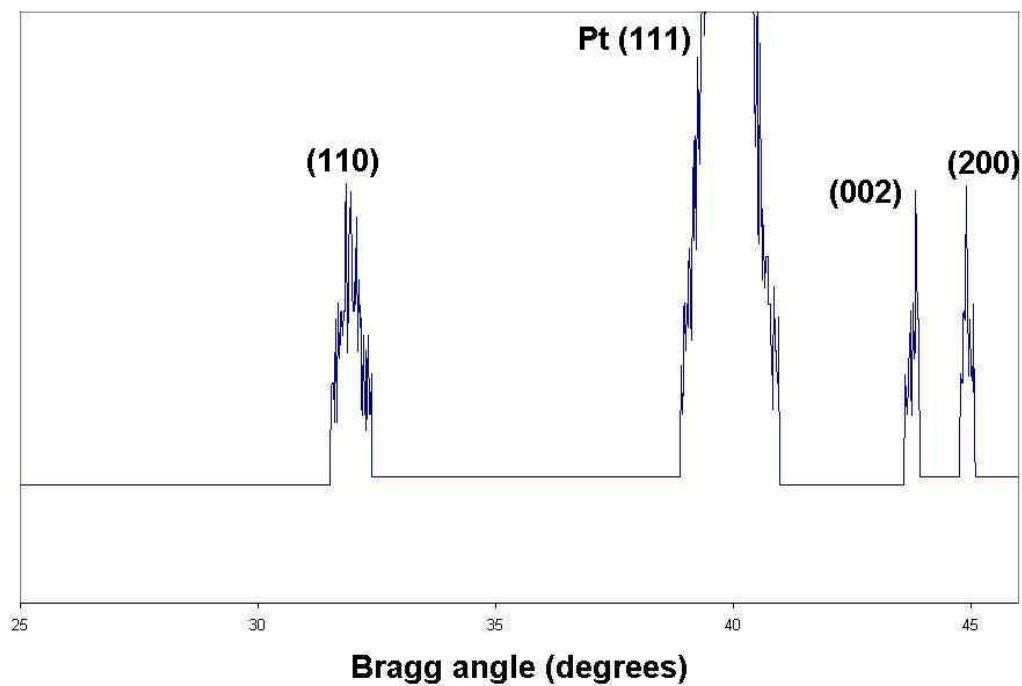


Fig. 3.33: XRD plot for PZT/Ti/Si with RTP done using (750, 0.5) for a substrate-target distance of 3.5".

It can be observed from the above plots that for a substrate-target distance of 3.5", the PZT perovskite phase is preferentially oriented in the (110) direction with an annealing recipe of (650, 15), as can be observed from figure 3.31. For the other two annealing recipes, a more polycrystalline PZT film is obtained with the (110), (111) and the (200) peaks being equally prominent.

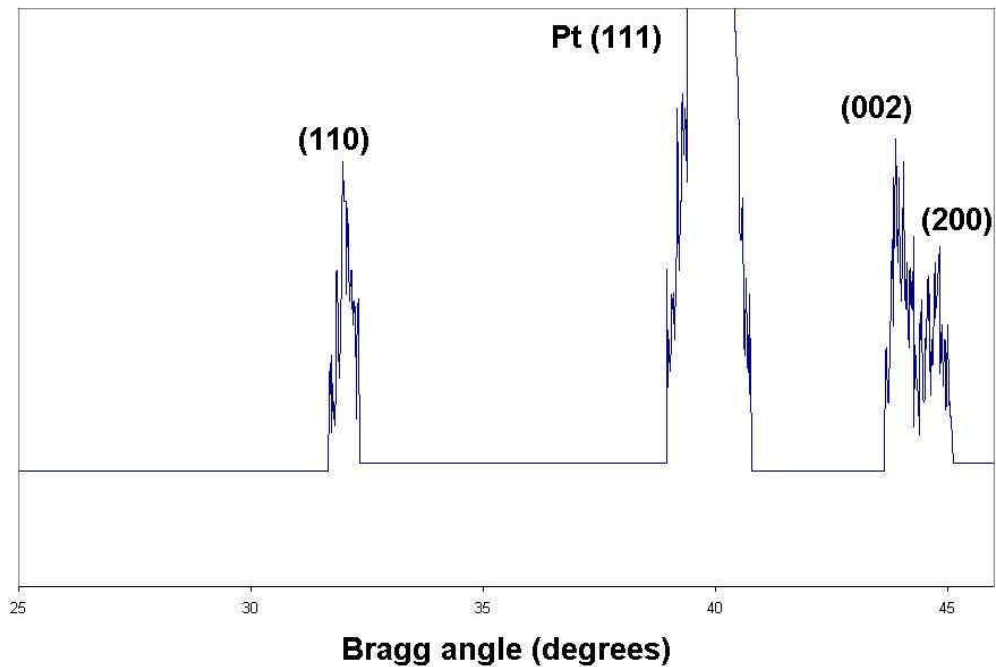


Fig. 3.34: XRD plot for PZT/Ti/Si with RTP done using (650, 15) for a substrate-target distance of 5".

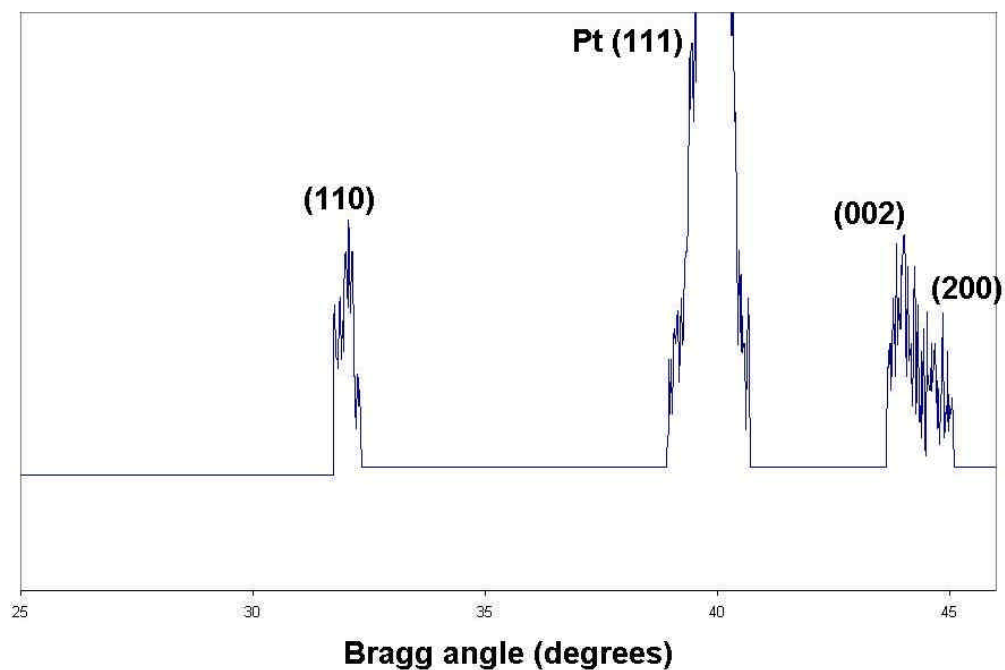


Fig. 3.35: XRD plot for PZT/Ti/Si with RTP done using (700, 5) for a substrate-target distance of 5".

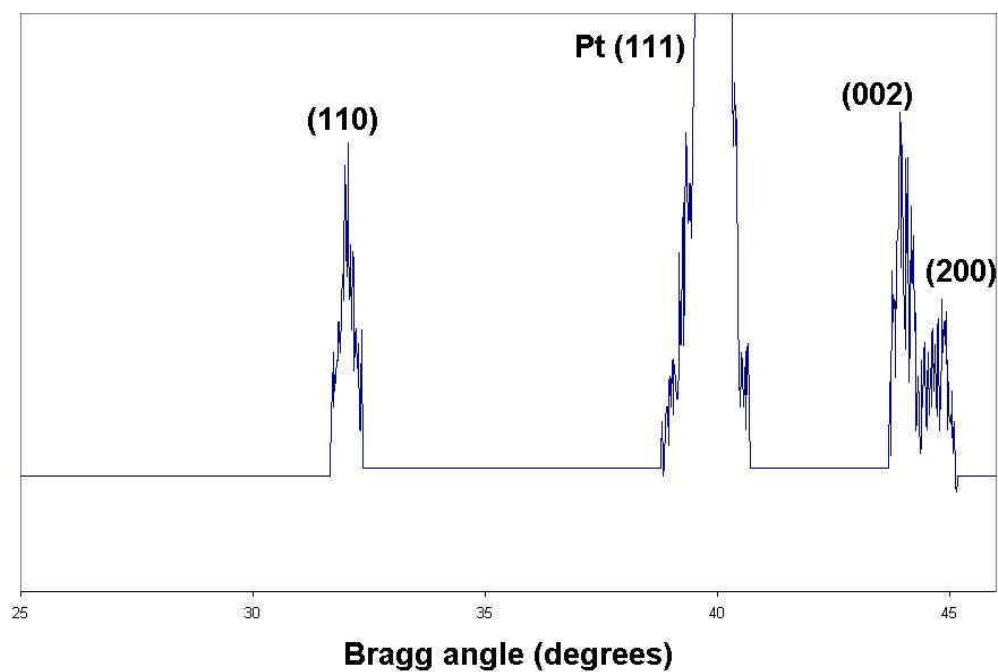


Fig. 3.36: XRD plot for PZT/Ti/Si with RTP done using (750, 0.5) for a substrate-target distance of 5".

The above plots for a substrate-target distance of 5'' show similar behavior for the (650, 15) and the (750, 0.5) annealing recipes, with the latter one showing a more crystalline nature of the PZT thin film, although it is not preferentially oriented.

On comparing all of the previous six plots, it should be noted that a higher crystallinity is obtained for a higher annealing temperature (750°C) and a shorter anneal time (30 seconds), irrespective of the substrate-target distance. However, preferred orientation is desired along with thicker films to avoid through-film shorting and to achieve enhanced piezoelectric response, and obtaining this requires higher sputtering pressures and reduction in the substrate-target distance.

The XRD plot below (Fig. 3.37) corresponds to sample 9 in table 3.4, where the substrate-target distance was reduced to 2.5''. An additional (101) peak is observed, but the (110) and (200) peaks remain prominent. Sputtering at this shorter substrate-target distance does give a thicker film as more of the plasma in the RF sputterer is now in contact with the wafer, but the quality of the film degrades. This was also confirmed after taking SEM pictures of the PZT/Pt/Ti/Si cross-section for different substrate-target distances. These have been provided below in figures 3.38 and 3.39.

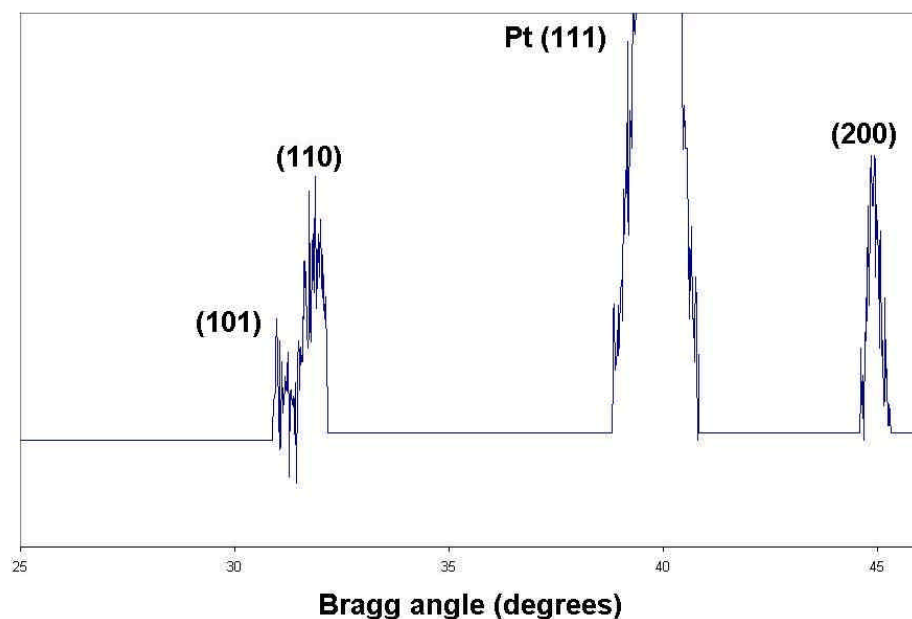


Fig. 3.37: XRD plot for PZT/Ti/Si with RTP done using (750, 0.5) for a substrate-target distance of 2.5".

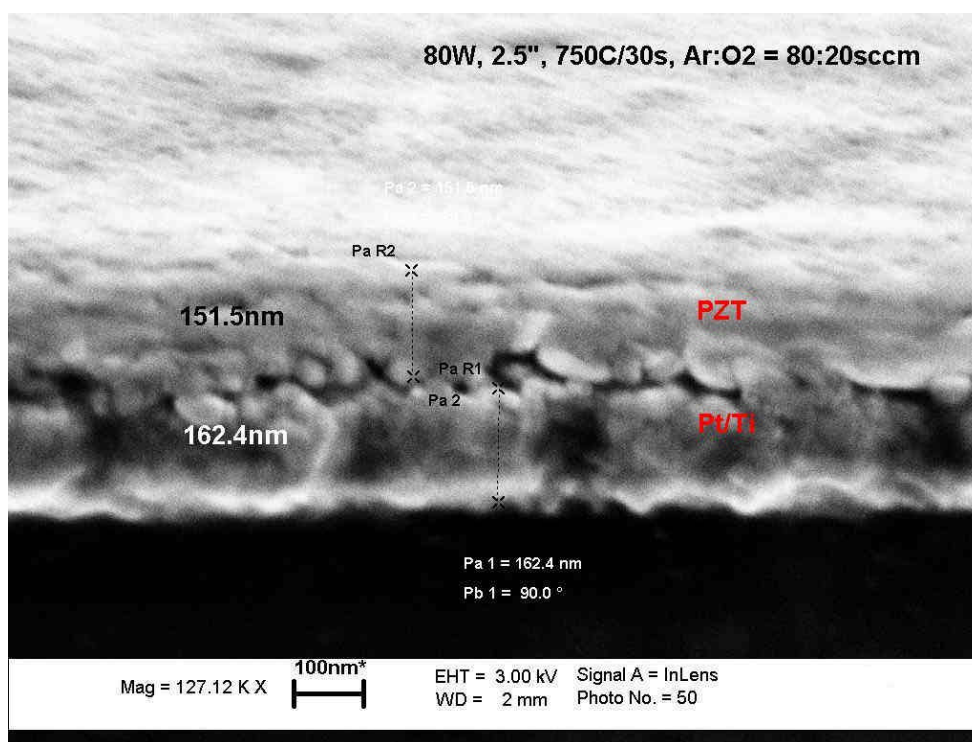


Fig. 3.38: An SEM cross-sectional view of PZT/Pt/Ti on silicon with a substrate-target distance of 2.5", annealed using (750, 0.5) recipe. Note the film roughness and the delamination observed at the PZT/metal interface. The film is about 150nm thick.

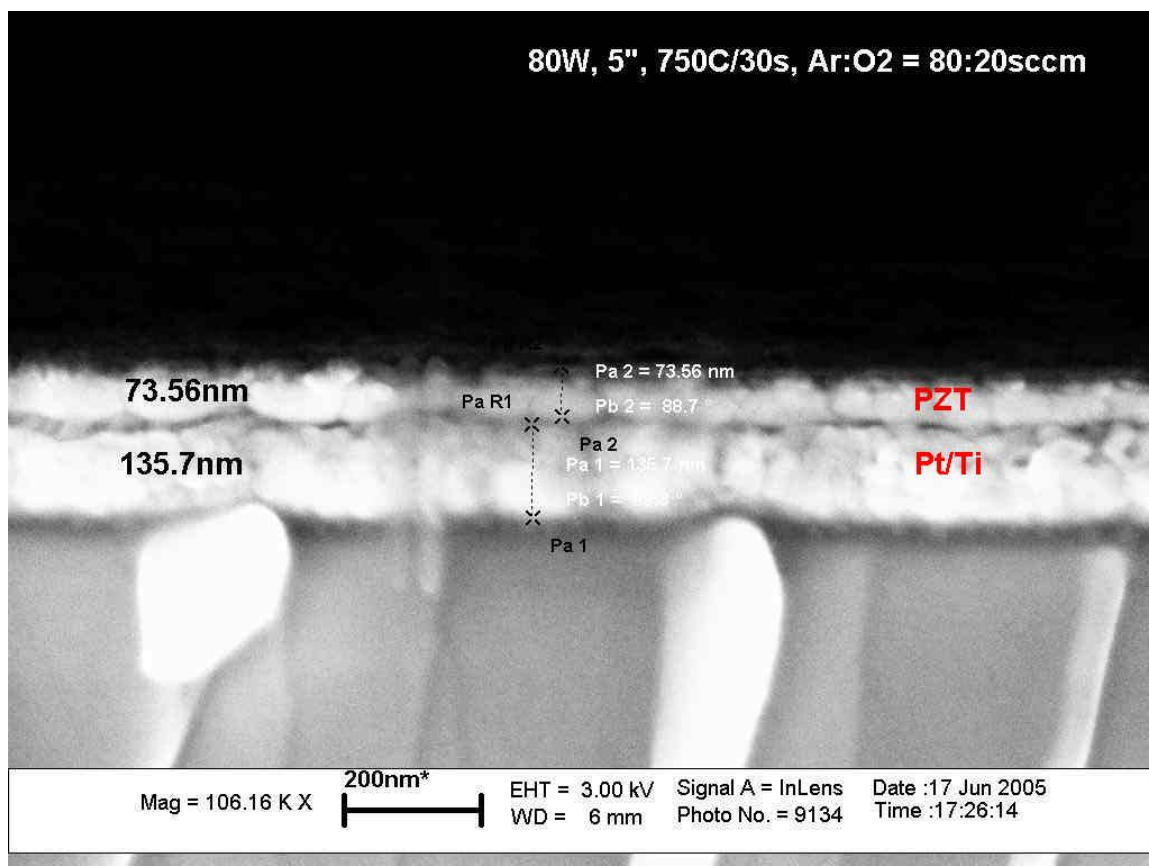


Fig. 3.39: An SEM cross-sectional view of PZT/Pt/Ti on silicon with a substrate-target distance of 5", annealed using (750, 0.5) recipe. Note that there is relatively lesser delamination at the PZT/metal interface, although it does exist. Also, the thickness of the film is about 74nm.

It can be deduced from the above discussion that there is a compromise between the PZT film quality and the film thickness using the current RF sputtering tool and RTP parameters. A better quality film is obtained for a larger substrate-target distance, but the thickness is less. The problem with a PZT film thickness of less than 100nm is that when such a film is incorporated in to a piezoelectric MEM resonator and wire-bonded for testing, the bonds break the film and cause shorting between the top electrode and the ground plane. This has been a recurring problem with many of the previous batches fabricated with thinner PZT layers of 50nm or less.

On the other hand, a thicker film is obtained for a smaller substrate-target distance, but it shows a lot more delamination and surface roughness. The solution to this problem is going for a higher sputtering pressure of 8Pa (or 60mTorr) with a 2.5" substrate-target distance. However, modifications will have to be made to the current RF sputtering tool to realize this. The other option is to further increase the power to 90W keeping the distance at a large value. There is the risk of damage to the target though.

3.3.3 Wet and dry etching of PZT

Etching of PZT is required when making the etch-pits in the thin film for obtaining access to the ground plane. Extensive characterization of both dry and wet etching of PZT was carried out.

In any resonator design, dry etching is always the preferred method over wet etching. This is because dry etching is usually a highly anisotropic process, and this prevents excessive undercutting of the smaller features. The advantage of wet etching is that it is a low cost process when compared to dry etching.

Dry etching of PZT in the RIE

Dry etching is usually done in a Reactive Ion Etcher (RIE) or in an Inductively-Coupled Plasma (ICP) etcher. The ICP usually has a much higher etch rate because it is capable of handling higher power and can be used for etching a wide variety of materials from oxides to metals. Extremely high-aspect ratio trenches can also be etched using the ICP. The RIE is also equally useful, and is usually preferred for dry etching of dielectrics. The gases required for dry etching PZT were available in the RIE, and so that was the preferred equipment.

It must first be noted that both fluorine and chlorine based plasmas have been researched in the literature for dry etching PZT. F-based plasmas give good selectivity but the process leaves polymer residues, while Cl-based gives clean etches but with poor selectivity. In our case, selectivity is very important for two reasons. One, we do not have

the option of using very thick photoresist layers because our features have small dimensions, and two; we do not have the option of using metal masking layers. It is for this reason that F-based plasmas suit our purpose better.

SF₆ has been reported [29] to be a good etchant for PZT. The etch recipe tried out is given below in table 3.5.

Table 3.5: RIE parameters for dry etching PZT/Ti/Si using SF₆

<u>Parameter</u>	<u>Value</u>
Plasma	SF ₆
Power	150W
Flow rate	15 sccm
Base pressure	15 mTorr

The etch rate for the above recipe turned out to be very less, and on over-exposure to the SF₆ plasma, even the silicon substrate got affected as SF₆ is an etchant for silicon.

Other reported methods for etching PZT are given below.

- CHF₃/Ar plasma also etches PZT according to Peng *et al.* [30]. They have used a gas mixture of CHF₃/Ar (70/30) with a total flow rate of 30 sccm and a power level of 150W. These parameters will give an etch rate of about 25 Å/min

- In another article, Shibata *et al.* [31] have patterned PZT thin films using the top Pt electrode as an etch mask. They have also used only SF₆ plasma, and obtained an etch rate of 200 Å/min at 400W and a flow rate of 2 sccm.

The second recipe was not tried out, because as mentioned before, SF₆ affects silicon as well. Also, the power level for this recipe is very high at 400W and this will affect the wafer.

Pure CHF₃ plasma was tried out without any Argon. The recipe is given below is table 3.6.

Table 3.6: RIE parameters for dry etching PZT/Ti/Si using CHF₃

<u>Parameter</u>	<u>Value</u>
Plasma	CHF ₃
Power	150W
Flow rate	30 sccm
Base pressure	10 mTorr

This gave a reasonable etch rate of about 50Å/min. The next thing characterized was the effect of CHF₃ on photoresist. SC1813 was spun on a test wafer with PZT/Pt/Ti/Si and patterned using the “Piezo” mask. This was put in the RIE and the process was run using the same parameters as above in table 3.6, except that the power was changed to 200W

this time to facilitate a faster etch. The change in the thickness of the resist along with time is given below in table 3.7.

Table 3.7: Thickness variation of the resist with RIE etch time

<u>RIE etch time (mins.)</u>	<u>Resist thickness (μm)</u>
0	1.961
5	No change
10	1.879
15	No change
20	No change
25	No change
35	1.75

It can be clearly seen from the above table that CHF_3 does not have much effect on photoresist. This is an excellent quality of CHF_3 , as it can be used as a good etch mask in the RIE. Also, as the resist thickness is not much, the smaller features can also be obtained. It was however observed that the smallest of devices did get affected, and the resist from the traces and some device structures were also gone. Most of the devices, however, were in very good condition.

Argon was also later introduced into the plasma in the RIE for dry etching PZT. The recipe used is as given below in table 3.8.

Table 3.8: RIE parameters for dry etching PZT/Ti/Si using CHF₃/Ar

<u>Parameter</u>	<u>Value</u>
Gases	CHF ₃ and Ar
Flow rates	21 and 9 sccm respectively
Power	150W
Base pressure	15mT

A significant amount of undercut was observed after etching. The undercut could be because of the presence of argon. Argon being an inert gas can only cause etching by bombardment and physical removal of the atoms of the film through a process known as ion milling. It is possible that the argon ions bombarded the PZT more than the fluorine ions, and so the undercutting was aggravated with the use of argon. On the other hand, CHF₃ etched off the PZT quite cleanly.

It can therefore be concluded that pure CHF₃ plasma is a good dry etchant for thin films of PZT, although the etch rate is rather slow because of the power limitation. If the power can be increased to beyond 400W, then it is a viable option. Addition of argon to the etch plasma in limited quantities is beneficial, but too much of argon will cause undercutting of the resist due to the ion milling effect.

Wet etching of PZT

In order to obtain higher etch rates, wet etching of PZT was also characterized. The primary constituents of a wet etch recipe for PZT contains HF, HCl and DI water in varying proportions. Other variants to this also use buffered oxide etch (BOE) instead of HF.

Table 3.9 below summarizes all the wet etching recipes tried out, along with the results of etching.

Table 3.9: PZT wet etch recipes

<u>Chemicals</u>	<u>Comments</u>
49%HF (1%) + HCl (24%) + DI water (75%)	This is an extremely fast etchant, and undercut the photoresist mask layer a significant amount.
BOE (6:1) + DI water	This showed a reasonable etch rate, although undercutting was still observed.
HCl (~6%) + DI water + few drops of 49%HF	This proved to be the best etchant and showed an etch process with visibly diminishing PZT. This allows for better control over the etching and therefore undercut of the resist mask layer can be avoided.

It was mentioned previously that the PZT layer is stressed. This was confirmed by using a strong etchant (such as the first recipe mentioned above in table 3.9) and observing the PZT under a SEM. The pictures taken are given below in figure 3.40.

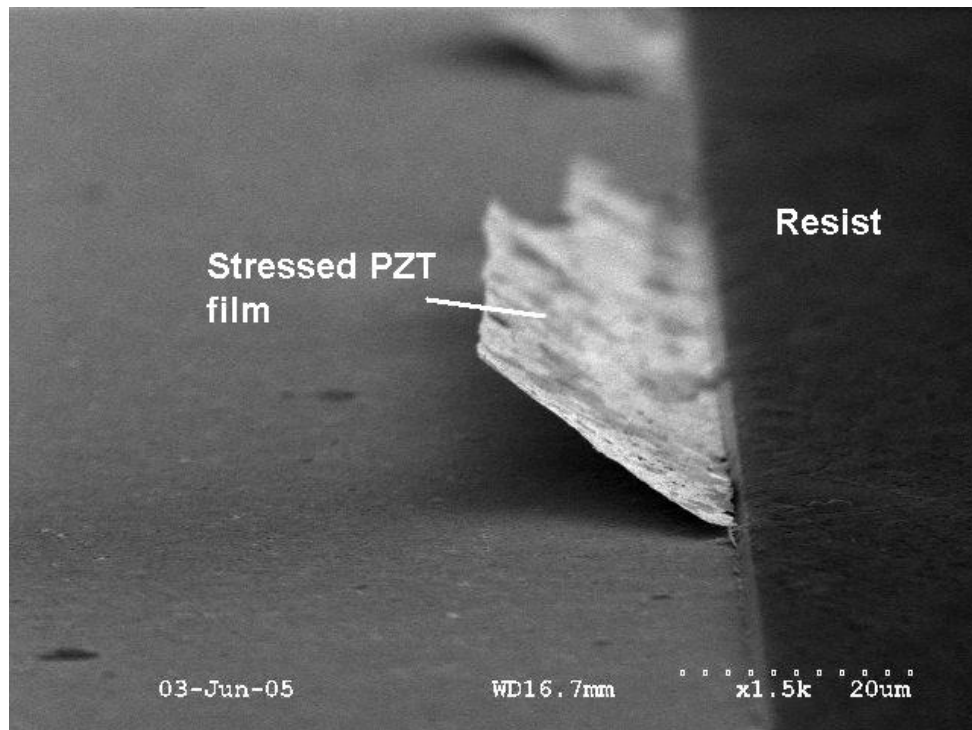
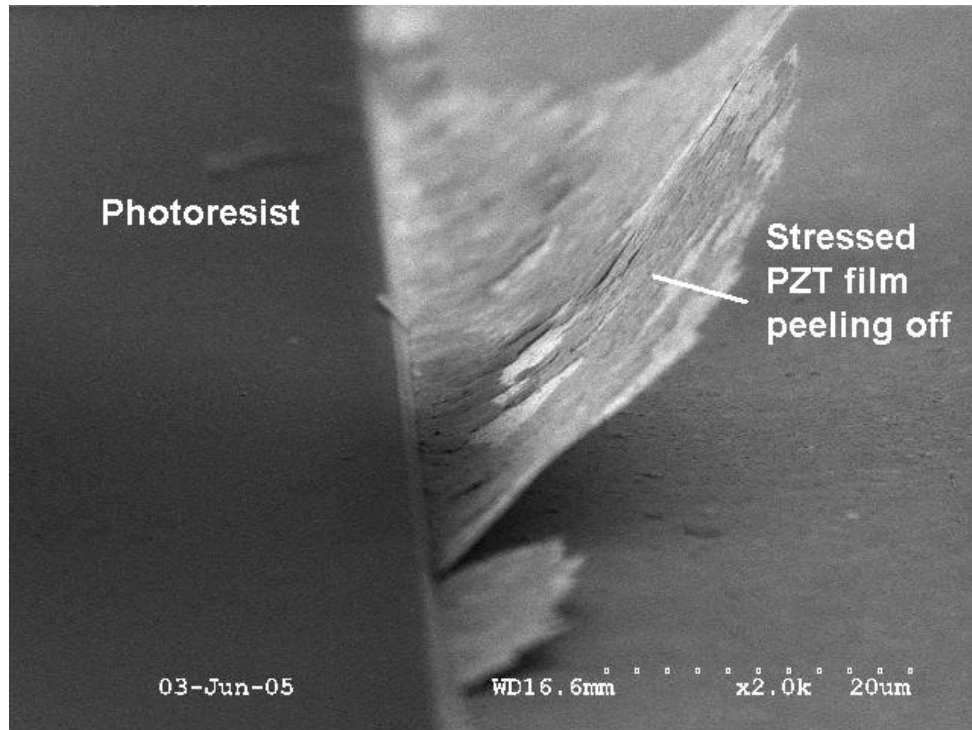


Figure 3.40: SEM pictures showing the peeling off of the PZT thin film on subjecting to a strong etchant. The stress in the film causes it to buckle upwards after delamination.

3.3.4 TiO_x diffusion-barrier layer characterization

The stack of layers forming a PZT-based MEM resonator is Pt/PZT/Pt/Ti/Si. However, it has been reported that if Pt is deposited directly onto silicon, there will be diffusion of lead contained in the PZT layer through the Pt and to the silicon layer. This will result in silicates being formed [12, 13], and this is detrimental in two ways:

- There will a Pb deficiency in the within the PZT film, thus changing its properties and characteristics.
- The silicates will melt at temperatures above 700°C, thus causing delamination of the overlying layers. [14]

It is for the above reasons that a diffusion barrier layer is employed between the Pt and the silicon. TiO_x is the choice for this layer because of its ease of fabrication and also because the diffusivity of Pt and Si is the lowest in TiO_x. A thin layer of Ti is usually again deposited on the barrier layer for better adhesion of the Pt. The characterization of this layer is given below in table

Table 3.10: TiO_x diffusion barrier layer parameters

Process	Process parameters	Desired thickness
Initial titanium deposition	E-beam evaporation	200nm
Oxidation of titanium [15]	Rapid thermal oxidation Temperature = 700°C Time = 10 mins.	350nm

However, it was later noticed that devices which require a reliable diffusion barrier layer are those which have a SiO_2 substrate. For the purpose of this project, a silicon substrate is being used, and so a thicker titanium layer between the ground platinum and the device layer silicon of the SOI can be considered to be a reasonably robust barrier layer.

3.3.5 Issues with patterning of platinum electrodes

The need for patterning the top platinum electrode was established as being imperative because the e-beam evaporator unit cannot really be trusted to give a uniform coat. The process which was used previously relied on the fact that the e-beam evaporation being non-conformal would not cover the sides of the PZT thin film. This would automatically provide a step between the top and bottom electrodes, thus allowing for the production of an electric field when a voltage is applied between the electrodes. However, the thin PZT film makes the task a lot tougher. The sample has to be exactly flat on the holder inside the e-beam otherwise the electrodes will be shorted, which was indeed the case with a fabricated batch of devices. If the top electrode could somehow be patterned, then this will not be an issue at all.

There are two ways in which the top Pt can be patterned:

- Use of negative resist and performing lift-off
- Dry/wet etching the top Pt

The first process was previously ruled out due to various reasons. Firstly, lift-off is not a very clean process and leaves a lot of junk lying around on the devices. Secondly, the

developing and use of negative resist has not been characterized properly, and its use always has created problems for previous users. Thirdly, and most importantly, during lift-off the wafer will have to be placed in an ultrasonic bath for stirring. Since the release of the devices has already been done much before any processing, the vibrations in the bath will cause the devices to break off. This was seen in one of the SOIs processed previously, and so that is not a good option.

As for wet etching of Pt, that also poses a problem. This is because Pt is a very robust metal and does not react easily to most etchants. Therefore, very strong etchants have to be used to etch it, and this will almost certainly etch off the PZT layer underneath very quickly as soon as it goes through the Pt layer. One platinum wet etchant is H_2O : Aqua Regia (1:1), while one for PZT has no more than 1-5% HF in H_2O . Therefore, it is clear that wet etching is not a valid solution.

That leaves the possibility of dry etching. Dry etching of Pt can be done using ion-milling. Since we do not have any ion milling equipment here, it was believed that the RIE could be used as one itself. Argon plasma can remove Pt via bombardment, i.e. there is no reaction as such going on for the removal of Pt.

A few recipes for the same were developed in the RIE. Using only pure Ar (or an Ar/ O_2 mixture), it has been shown in the literature that Pt ion milling can be done quite effectively. However, a high power ($\sim 700\text{W}$) and really low pressure ($\sim 3.5 \times 10^{-4}$ torr) was used for such a process, both of which are not possible with the RIE unit in the clean

room here. However, TiN or Ti hard masks have been used with such high power levels, while as in our case photoresist was used as a masking layer. Therefore, a power of 300W and a pressure of 10-30 mTorr were thought to be enough. Oxygen gas has also been used as a passivating gas in the literature along with Ar. O₂ would not be required in our case because there are no metal hard masks being used. Oxygen forms a passive oxide layer with the metal mask, thus preventing it from being attacked by the ion beam and thereby improving the selectivity of Pt.

The following recipes for the ion milling of Pt were tried out in the RIE.

Table 3.11: Pt etching using ion milling – recipe 1

<u>Parameter</u>	<u>Value</u>
Gases used	Ar
Flow rate	20 sccm
Power	300W
Base pressure	20 mTorr

Table 3.12: Pt etching using ion milling – recipe 2

<u>Parameter</u>	<u>Value</u>
Gases used	Ar + O ₂
Flow rate	20 sccm + 32 sccm
Power	300W
Base pressure	20 mTorr

Unfortunately, none of these had much effect on platinum, and the resist, even on hard-baking, would be milled off before platinum. This was because the power was too low in this case, causing the etch rate for platinum to be very slow.

The only solution seemed to be using negative resist and lift-off to pattern the top electrode. Extensive characterization of the negative resist NR7-1500P was done and the details are provided below.

A number of test wafers were spun with negative resist NR7-1500P and different exposure times, post-exposure bake times, and developing times were examined. After a lot of trials, a good recipe was obtained which did not have any problems that were occurring before. There were no bent or curved features, because excessive primer (HMDS) was used. Also, a thickness of $\sim 2.75\mu\text{m}$ was spun, so that the lift-off process could be carried out effectively. The parameters are summarized below.

Table 3.13: Parameters for negative resist patterning

<u>Parameter</u>	<u>Value</u>
Resist used	NR7-1500P
Spin rpm/time	1000 rpm/40s.
Thickness of resist obtained	$\sim 2.75\mu\text{m}$ (good for the lift-off process)
Exposure time in the MA-6	33s. (365nm wavelength)
Developing time	40s. in RD6

The actual reported energy required for 1500P is 21mJ/ μm of resist, which comes out to an exposure time of about 24s. with the lamp intensity set at about 2.5mJ/s. It is clear that a lot of over-exposure is being given to the resist. This is done mainly for two reasons:

- It is observed that no curved features and/or broken features are obtained when this over-exposure is given.
- Previously, there was this problem of losing the smallest (1 μm) features when positive resist was being used. We do not have this problem here, as over-exposing negative resist will only mean that the 1 μm traces will now open up to be much wider. This is advantageous because it also compensates for any misalignment that may be present.

However, over-exposing negative resist also has some disadvantages. There are certain electrode shapes on disc and block resonators which have very small gaps between the input and output electrodes. Over-exposing results in these gaps getting closed up, and therefore these devices are rendered non-functional due to short between the two electrodes. But most of the simplest block resonators and some disc-shaped ones develop well, and these include the smallest devices also. Therefore, it is these devices which have been targeted in all the batches.

Therefore, lower exposure times (30-35s) result in the features in the 10 μm and 20 μm discs and blocks to develop well, but the larger devices have curved or lost features. However, overexposing gives all of the larger devices but the 10 μm device features “close up” and are lost.

Lift-off for the top Pt electrode

The parameters for patterning the negative resist have been noted in table 3.13 above. After getting the pattern transferred to the wafer, the next crucial step is the lift-off of the Pt.

Although in principle, lift-off is a very simple process, it turned out to be a challenging task in practice. This is mainly because lift-off is a very physical process, and involves stripping of the resist to give a pattern below. In our case, the top “Piezo” mask was being used for both the piezoelectric and top electrode layers. The mask is a clear field one, and therefore was not designed to be used for lift-off. It was designed keeping in mind that all the layers will be patterned by etching. This posed a problem, because now a lot of resist has to be removed from the wafer during lift-off. This implies that more debris and residues will be remaining on the devices, and obtaining clean devices will be a challenge.

A lot of characterization was done for simulating the lift-off on test wafers. Different thicknesses of Ti (for better adhesion) and Pt were evaporated on bare silicon wafers patterned with NR7-1500P. Lift-off was carried out using different solvents with or without ultrasonic shaking. When the shaker was used, it gave a much cleaner process, as expected. But, this same process cannot be used for the already released devices when processing SOI wafers. The shaker is powerful enough to break the devices, which is undesirable. This is shown in figure 3.41 below.

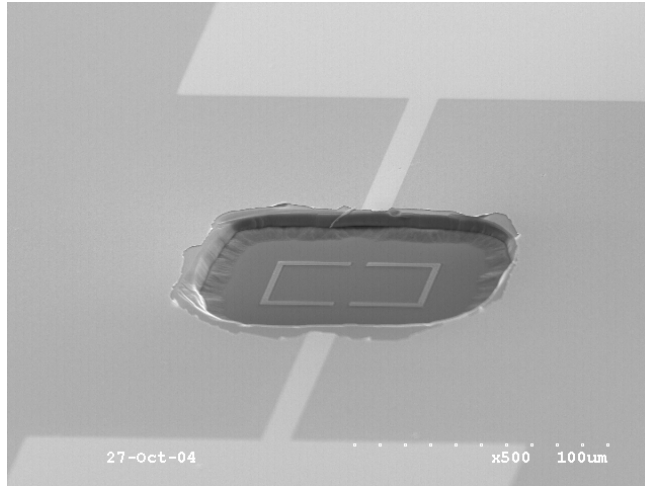


Figure 3.41: This is the result of doing lift-off using the ultrasonic shaker for long periods of time. Devices started breaking off after only a 5-second dip in the shaker liquid.

The solution to this problem was firstly, not to use the shaker for long times, typically not more than a 2-second dip. If the shaker use is completely eliminated for the lift-off process, then the other alternative is to put the wafer *upside down* in acetone while stripping of the resist. This will help the resist and metal being stripped off to fall to the bottom and not mess up the wafer. This was carried out on an SOI wafer, and the result was satisfactory. However, due to lack of any tweezers or holding tools which could hold the wafer upside down, the wafer was held physically by hand using neoprene gloves for protection. It was shaken mildly in acetone and DI water alternately, acetone being used for resist stripping and the DI water for cleaning up the residues. This procedure took about 45-50 minutes to obtain a clean wafer with little or no residues remaining.

To assist further resist removal, the wafer was then placed in RR-4, the negative resist remover, at 60°C for 10 minutes. This showed some signs of improvement, but not much. It's not favorable to keep the wafer in RR-4 for very long, because the effect of the

remover on PZT is unknown. For instance, the positive resist remover is highly basic, and when devices with ZnO were placed in this remover for a long time, the ZnO also got etched off. Therefore, after 10 minutes in RR-4, the wafer was ashed in the RIE using oxygen plasma for another 10 minutes. This showed some significant improvement in the lift-off process.

From the above discussion it can be observed that the use of negative resist and lift-off is a very tedious and time-consuming process. The lithography tools in the clean room are not good enough to pattern 1 μ m features using negative resist. Alternatives had to be identified and employed. The reason why negative resist was being used was that we could not etch the top platinum electrode using conventional wet etching, and hence had to apply physical means (such as lift-off) to pattern it.

3.3.6 Implementation of gold electrode

It was found that Au/Cr top electrode can be a good alternative to platinum [24]. The distinct advantage of Au/Cr over Pt is that the wet etchants for both Cr and Au do not attack the underlying PZT layer. Therefore, the process can now be simplified to the following steps:

- Etch trenches and release the devices in HF.
- Evaporate the ground electrode Pt/Ti.
- RF sputter the PZT and post-anneal in the RTP.
- Evaporate chrome and gold all over.
- Pattern *positive resist* over the wafer using the “Piezo” mask.

- Etch through the gold layer first, and then the chrome layer using the appropriate wet etchants for each.
- Now use this Au/Cr as an etch mask for wet etching of PZT.

This was tried out on a test wafer. 1000Å of gold was deposited on to the silicon test wafer with 500Å of chrome as an adhesion layer. The stack of layers was Au/Cr/PZT/Pt/Ti/Si. The goal was to test the effect of the respective gold and chrome etchants on the underlying PZT layer, if any.

Resist SC1813 was then spun and patterned on the wafer using the “Piezo” mask. Gold was first etched using the purchased Transene Gold Etchant TFA. The etch rate as given by the manufacturer is 28Å/s, and therefore it would take about 35s. to etch off 1000Å of Au.

The gold etchant is a dark opaque liquid, and it is therefore difficult to see the wafer inside the beaker when immersed completely in the liquid. Due to this limited visibility, complete removal of the gold could not be ascertained after 35s. The wafer was kept inside the etchant for 1 minute instead and then removed, rinsed in DI water and blown dry. On observing the wafer, it was found that the etch rate was very consistent with the prescribed one (i.e. 28Å/s), and therefore the resist was undercut to a considerable extent. Most of the gold was lost underneath the thinner features. However, the etching was very uniform, and also did not affect the underlying chrome layer at all. To prevent undercutting during future processing, two methods can be employed:

- Keep the wafer immersed in the etchant for exactly the calculated time. If 35s. is what it takes for 1000Å, then only that much time must be given.
- Dilute the etchant with DI water to slow down the etch rate. 35s. is a short time and can lead to undercutting due to faulty removal of wafer because of human error. Diluting the etchant with, say, an equal part of DI water will double the etch time and will minimize errors due to hurrying up the process.

The next step was to etch the chrome layer and see if it had any effect on the PZT layer below. The previously patterned photoresist was used as an etch mask for the chrome layer also. Chrome etchant from Cyantek is provided by the clean room staff. This solution has an etch rate of 24Å/s as prescribed by the manufacturer. Therefore, 500Å of chrome would take about 20s. to etch off completely. This solution is a clear yellow one, and it is easier to view the wafer. The wafer was immersed for exactly 20s. in this solution, and on rinsing and blow drying showed proper etching of the chrome. However, because of the short etch time chrome was still present on certain undesirable parts on the wafer. Using a diluted etchant is again warranted in this case.

Nonetheless, the PZT remained unaffected throughout the etching. The chrome etchant does not attack PZT at all, and this is very much desirable. Therefore, employing this Au/Cr electrode is a viable method of eliminating the use of negative resist for the top electrode.

3.3.8 Current process flow for PZT-based MEM resonators

Figure 3.42 below shows a schematic of the steps currently being followed for the fabrication of PZT-based piezoelectric micromechanical resonators.

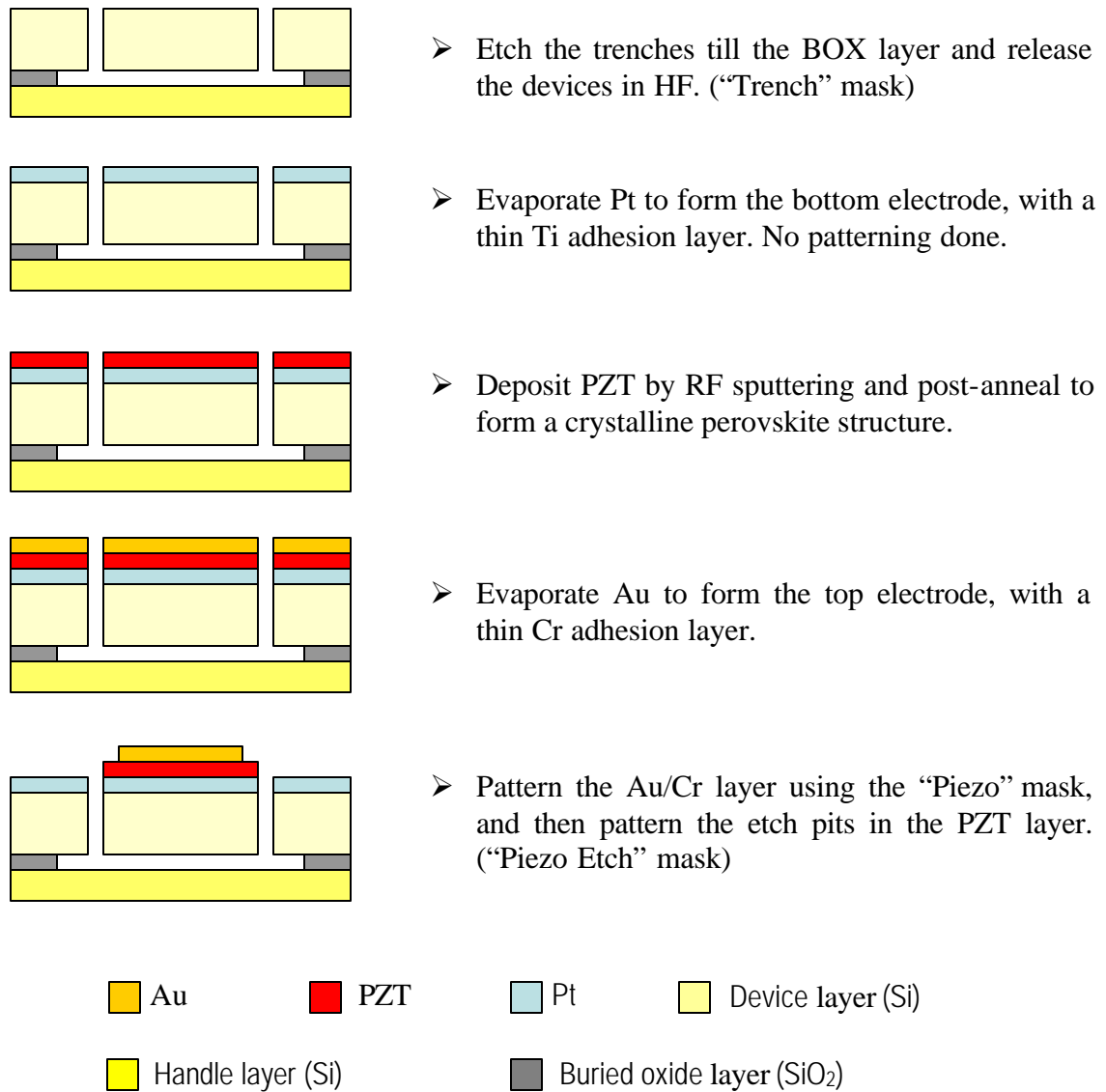


Figure 3.42: Process flow for fabrication of PZT-based MEM resonators

3.3.7 Challenges in PZT processing

In all the previous sections, the extensive characterization performed with respect to PZT-based MEM resonators has been outlined. It can be noted that replacement of ZnO with PZT is not a trivial task. Every single layer on the device has to be carefully processed otherwise it will cause delamination of the whole stack of layers besides giving rise to other complications. At many stages during this work, complete batches of PZT-based resonators were fabricated on silicon-on-insulator wafers with different process flows which took care of the previous problems. However, a successful batch could not be fabricated because of the daunting task of maintaining the quality of the PZT film throughout the fabrication. Almost every time, the top and ground electrodes came out to be shorted, either because the PZT layer was too thin, or it had a degraded quality allowing it to break when wire bonded.

The limitations in the Georgia Tech clean room have mainly to do with the RF sputterer and the RIE with regard to PZT processing. An increase in the sputtering pressure will allow for more robust films, and the low power level in the RIE does not allow for ion milling of the PZT, which has been established as a good anisotropic dry etch method to prevent undercut.

These modifications will allow for higher quality PZT films, and therefore realize RF-sputtered PZT-based MEM resonators.

CHAPTER 4

RESULTS

This chapter reports the frequency response obtained for ZnO-based two-port block resonators. The first section reports on results obtained from a batch with a high-resistivity ground plane. The second sections reports on the frequency response with a gold ground plane, and compares these with the previous results.

Testing was carried out in air as well as in vacuum to quantify the change in the quality factor. Since damping of the resonator occurs in air, the quality factor is lower than in vacuum. The frequency response was recorded using an Agilent 4395A network analyzer. The two pads on either side of the resonator, as shown below in figure 4.1, were wire-bonded and connected to the RF_{IN} and RF_{OUT} of the network analyzer.

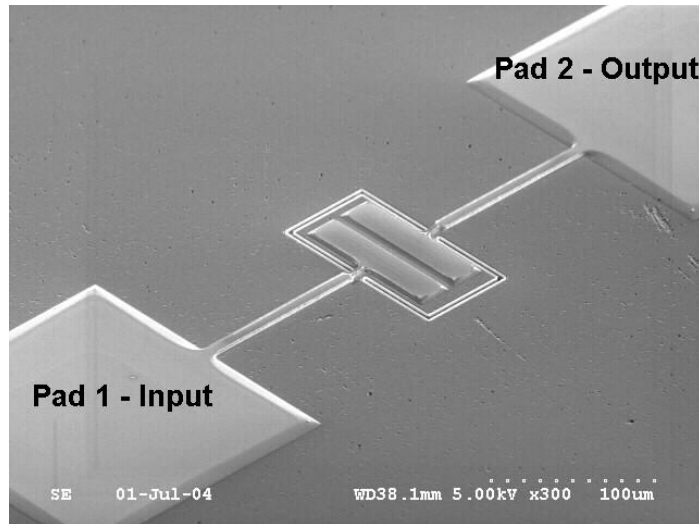


Fig. 4.1: A 60 μ m long block resonator showing the input and output pads

Alternating current passes from the one port to the other, and the response of the piezoelectric resonator, which is a part of this circuit, is recorded. A schematic of this setup is shown below in figure 4.2.

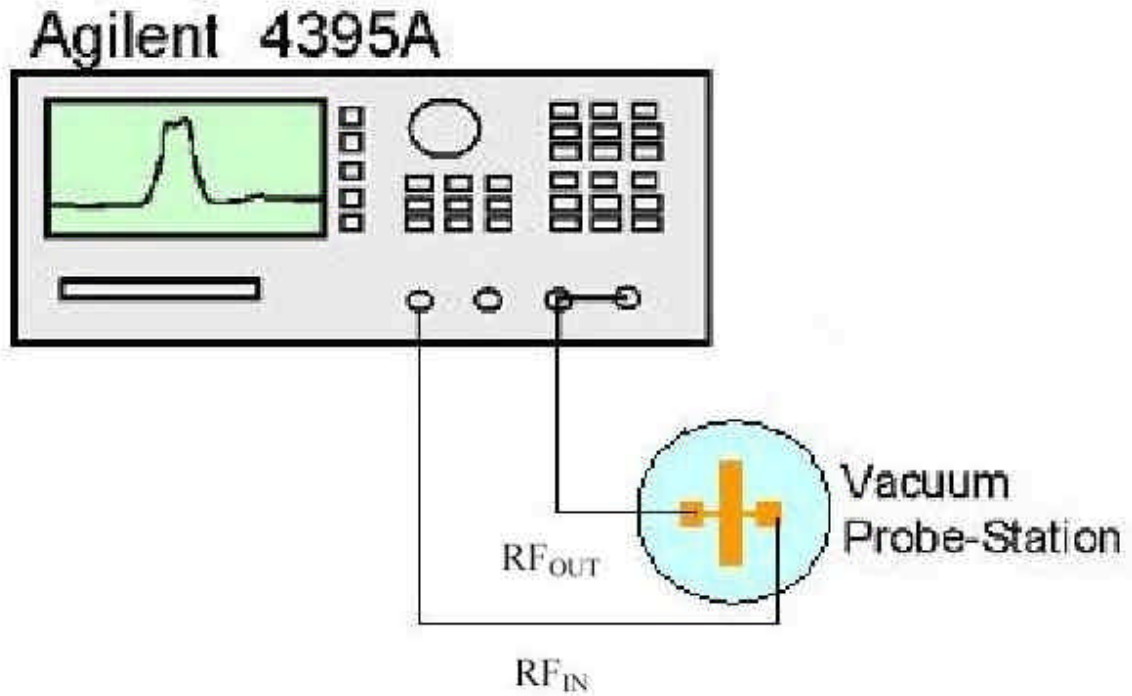


Fig. 4.2: A schematic of the setup for testing piezoelectric MEM resonators

4.1 FREQUENCY RESPONSE WITHOUT A GROUND PLANE

The devices in this batch have no metal ground plane. The resistivity of the ground plane is in the range of 1 to 2 kilo-ohms. Before presenting the measured results, the theoretical calculated frequencies as obtained from ANSYS simulations and basic resonator design calculations are provided below in table 4.1.

Table 4.1: Calculated frequencies for length-extensional block resonators

Length (μm)	1 st resonance mode (MHz)	3 rd mode (MHz)	5 th mode (MHz)
40	104	312	520
60	69.1	207	345.5
120	34.5	104	172.5
240	17.2	51.8	86
480	9	27	45

This table shows that the measured results presented below in figures 4.3 through 4.6 are in close agreement with the calculated frequencies.

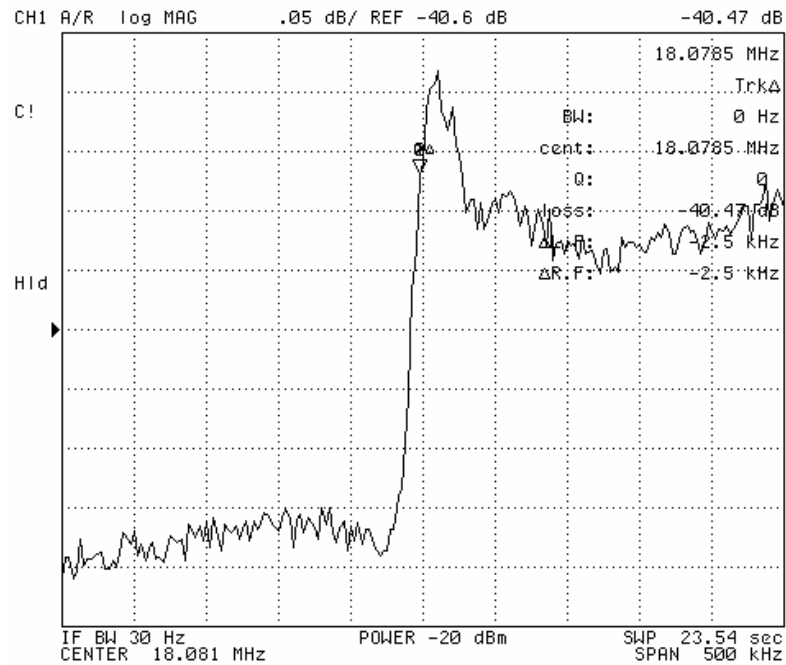


Fig. 4.3: 1st extensional mode of a 240 μm by 40 μm block resonator ($f_0 = 18.08\text{MHz}$)

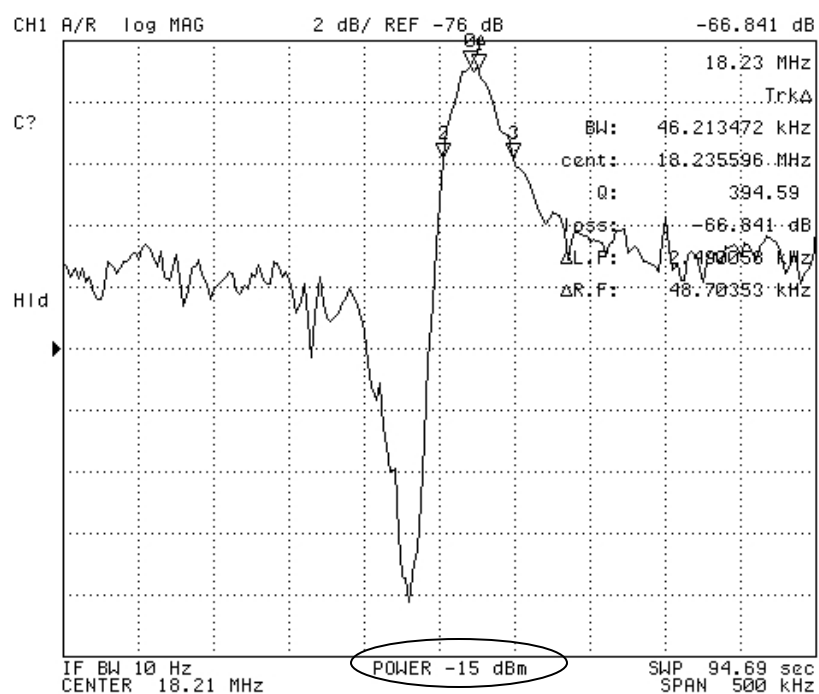
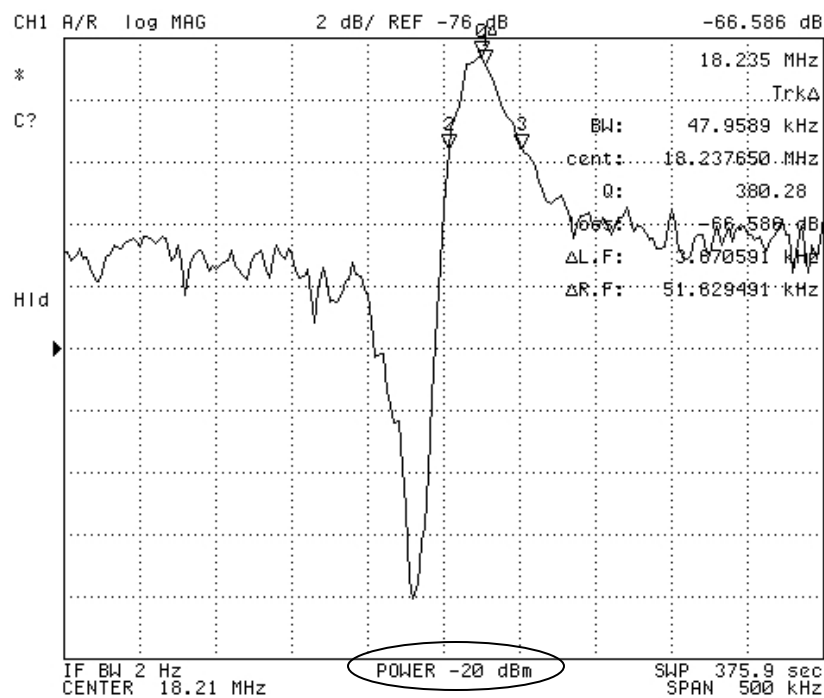


Fig. 4.4: Test of ZnO film quality with varying power; top is -20dBm, bottom is -15dBm; (240 μ mX40 μ m block resonator, f_0 =18.23MHz) (continued)

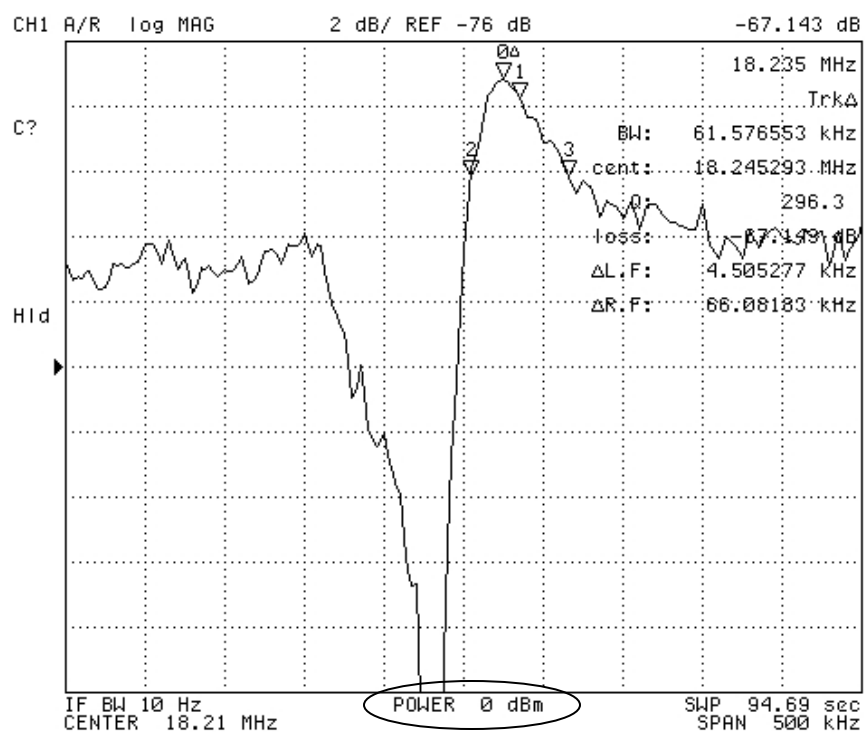
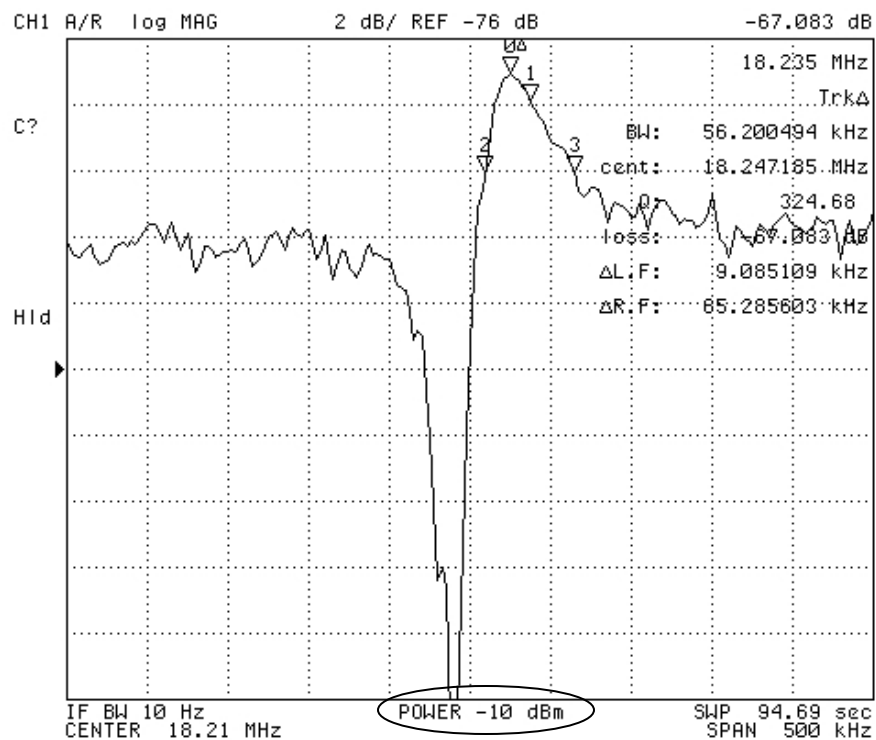


Fig. 4.4: Test of ZnO film quality with varying power top is -10dBm, bottom is 0dBm; (240 μ mX40 μ m block resonator, f_0 =18.23MHz)

The results above show that the ZnO film quality is considerably good. Changing the power from -20dBm (top left) to -15dBm (top right), and then to -10dBm and 0dBm (bottom left and right respectively) still shows similar response at the fundamental resonating frequency. This shows that the ZnO film as a dielectric is very stable.

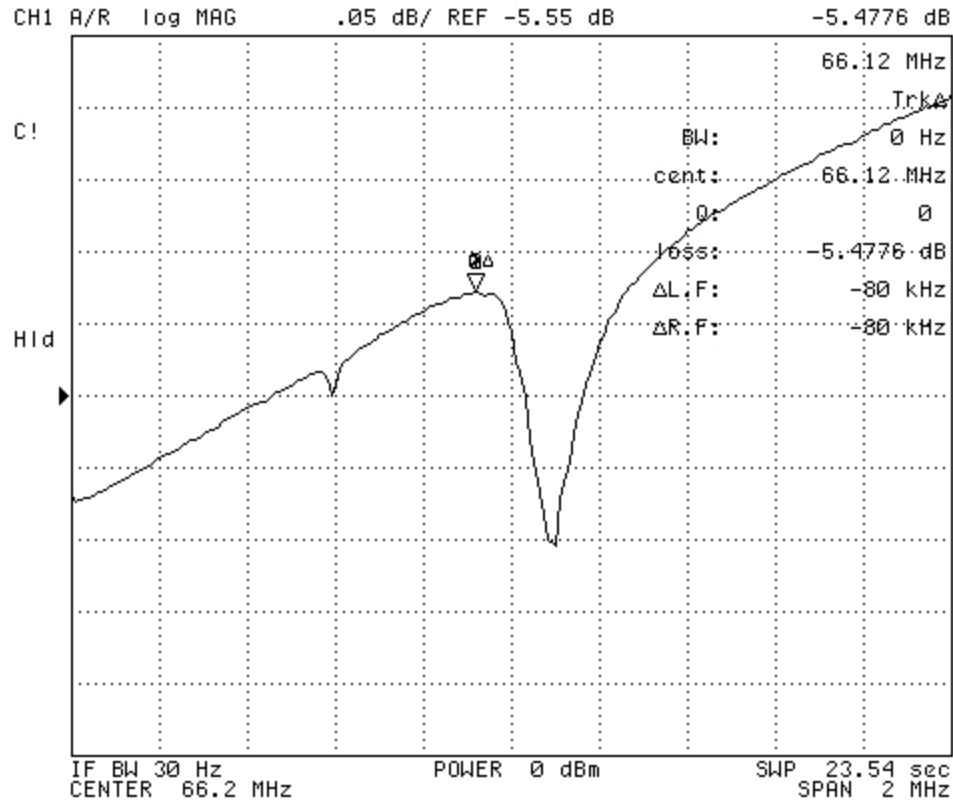


Fig. 4.5: 1st extensional mode of a 60 μ m by 30 μ m block resonator ($f_0 = 66.12$ MHz)

The feed-through capacitance (C_f) was partially cancelled in the above 60 μ m long resonator by putting a 220nH inductor in parallel with it. Figure 4.5 above shows only the anti-resonance peak and the resonance peak is eaten up by the noise created due to the C_f . Figure 4.6 below shows the result after cancellation.

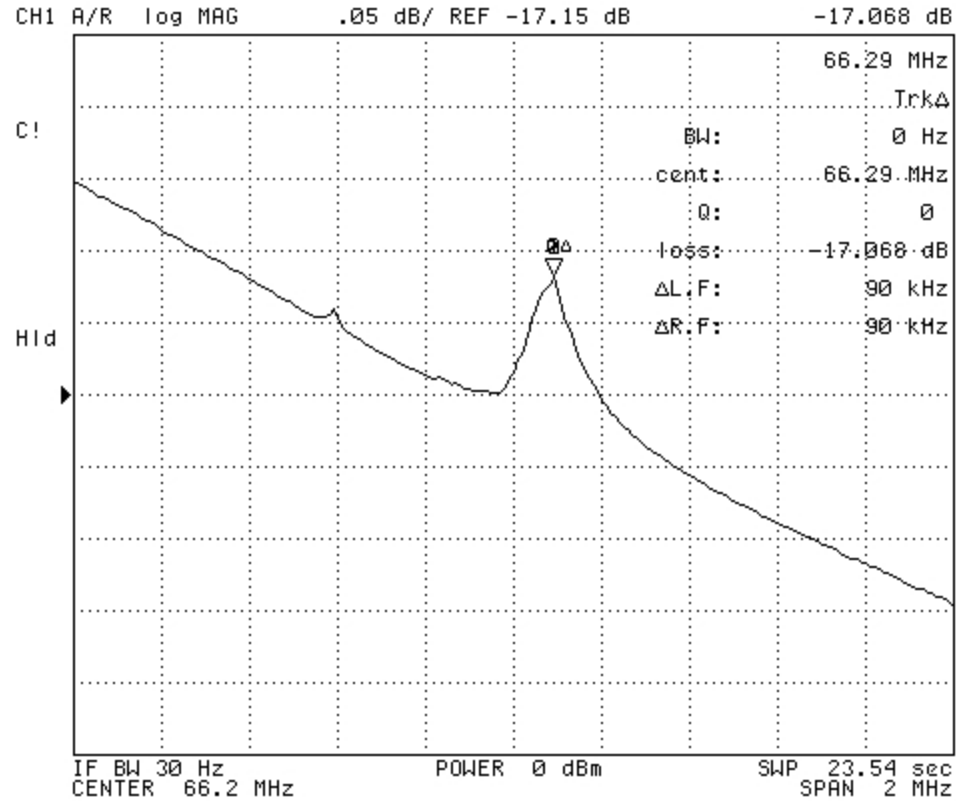


Fig. 4.6: Feed-through cancellation with 220nH inductor in parallel with C_f

4.2 FREQUENCY RESPONSE WITH A GOLD GROUND PLANE

The results below are from devices fabricated with a gold ground plane to reduce the feed-through level and increase the transduction from input to output giving a better frequency response. A SEM picture of a wire-bonded device showing the gold ground plane is given below in fig. 4.7. On comparing these results with the ones in the previous section, it is observed that the peaks are much cleaner in these devices due to the reduced noise level. Also, the quality factors are much higher with the highest obtained Q being 12400 for a 240 μ m long block resonator.

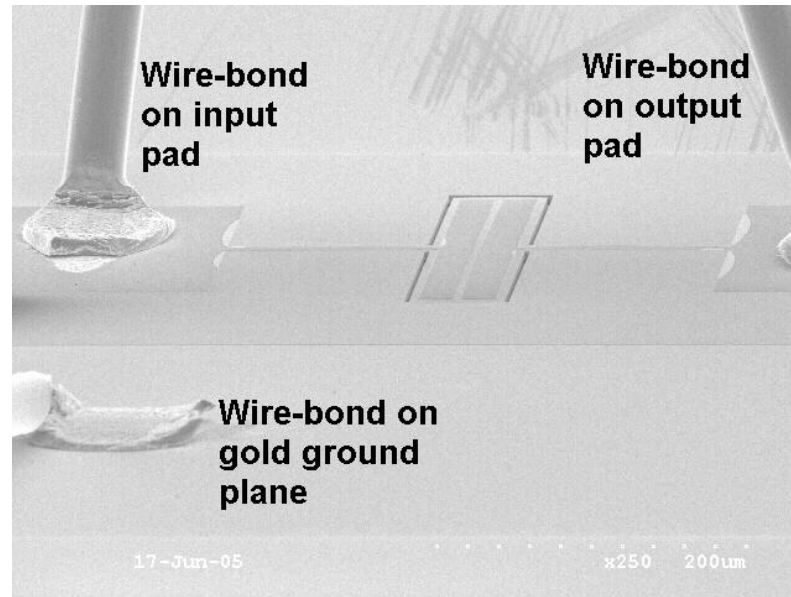


Fig. 4.7: A SEM picture showing a wire-bonded device with a gold ground plane

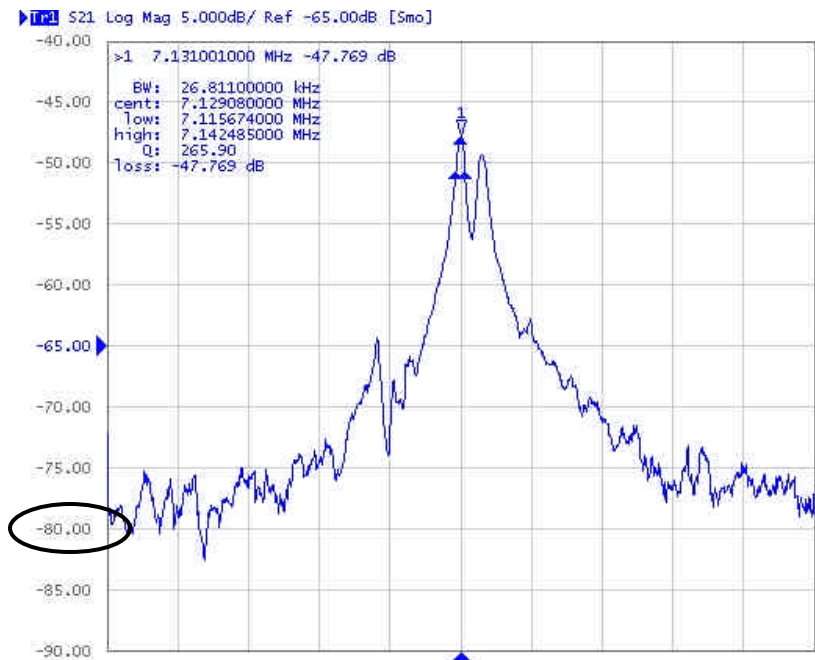


Fig. 4.8: The fundamental resonant mode for a 480μm by 40μm block resonator ($f_0 = 7.13\text{MHz}$). Note the feed-through (noise floor) level at -80dB. This is the lowest feed-through that has been obtained so far for any piezoelectric MEM resonator.

240 μ m by 40 μ m block resonator

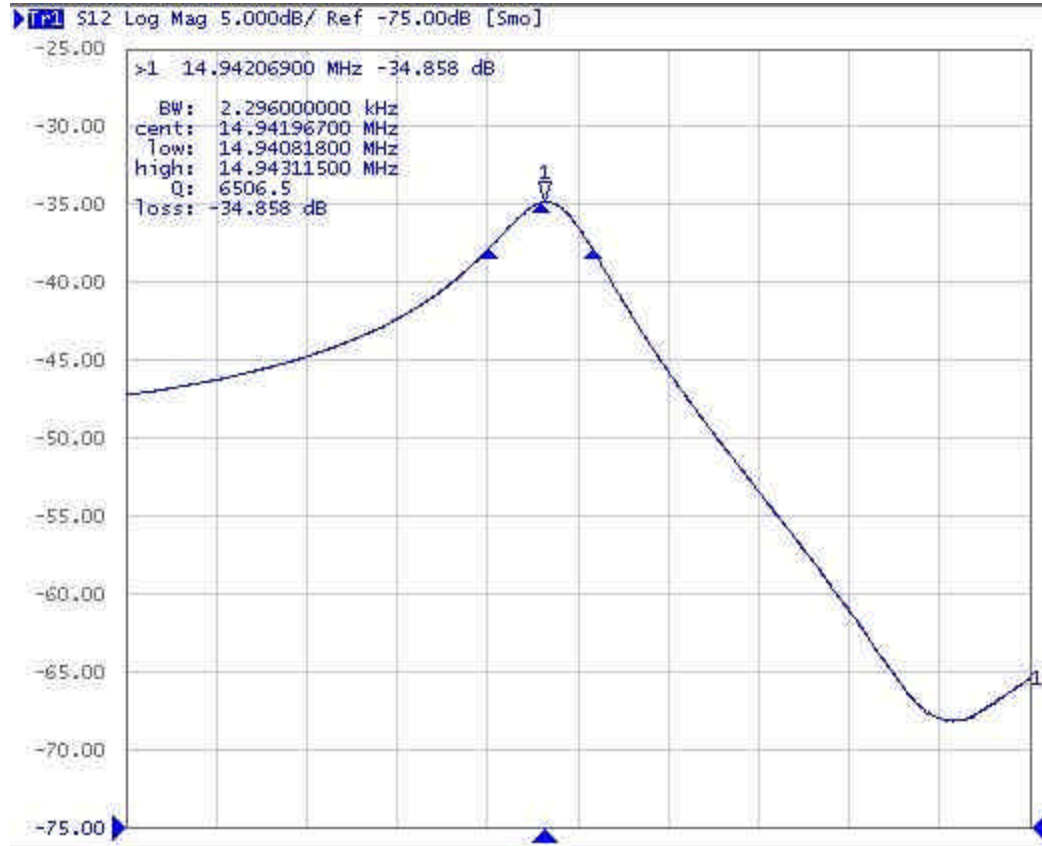


Fig. 4.9: At the fundamental resonant frequency in air, $f = 14.94\text{MHz}$, $Q=6500$

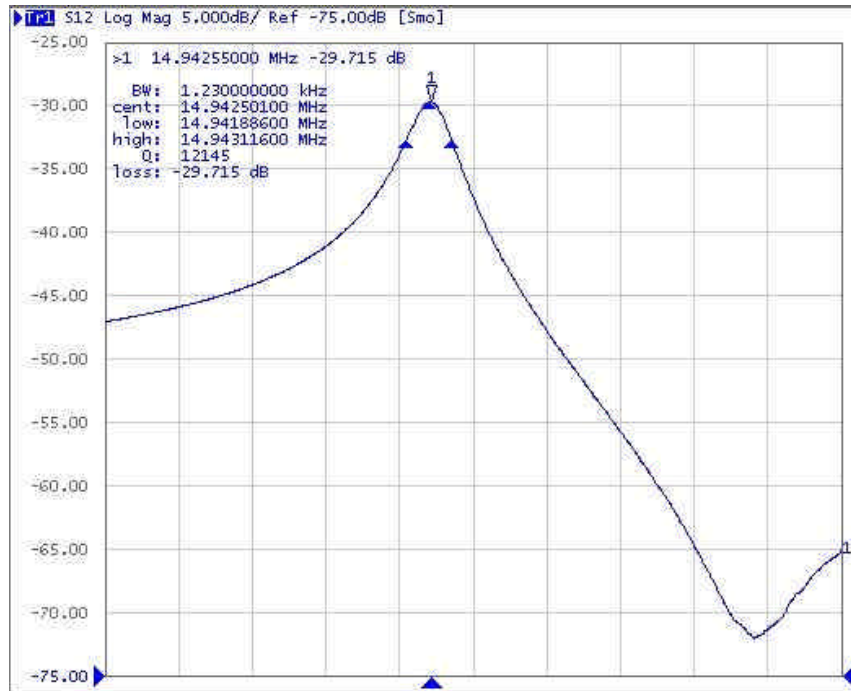


Fig. 4.10: At the fundamental resonant frequency in vacuum, $Q=12150$

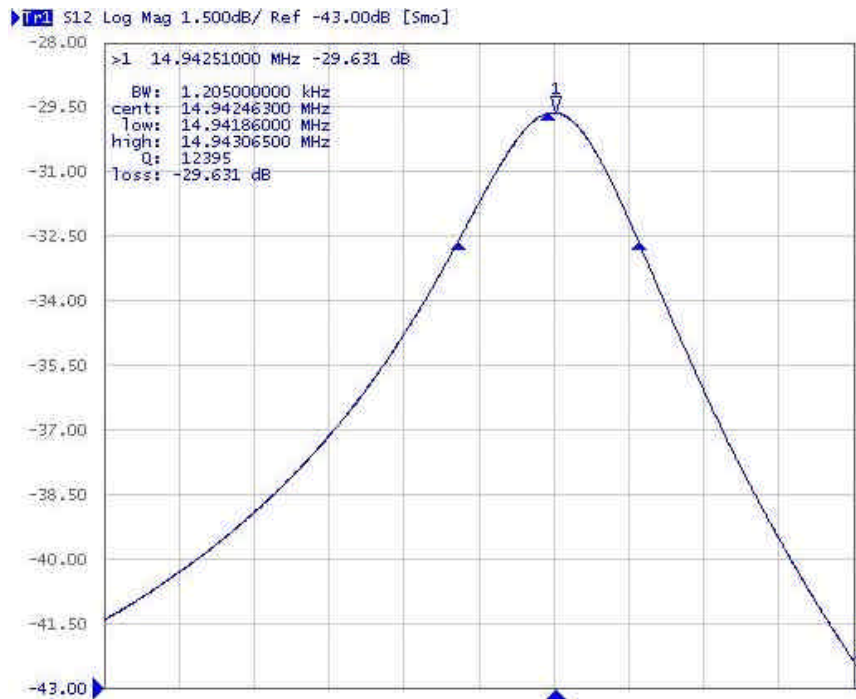


Fig. 4.11: At the fundamental resonant frequency in vacuum (showing only the resonance peak), $Q=12400$

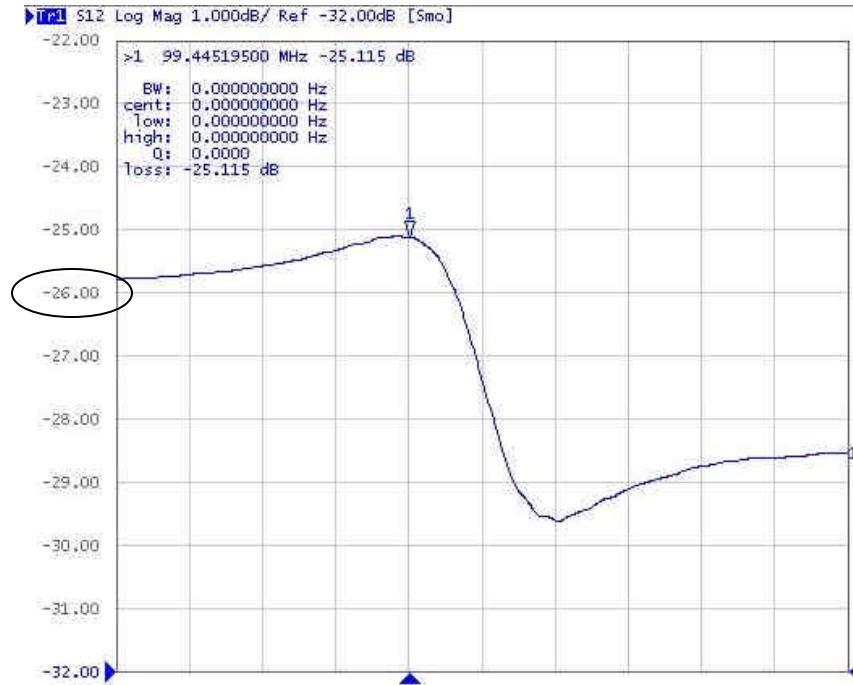


Fig. 4.12: At the 6th resonant mode in air, $f = 99.45\text{MHz}$, before calibration

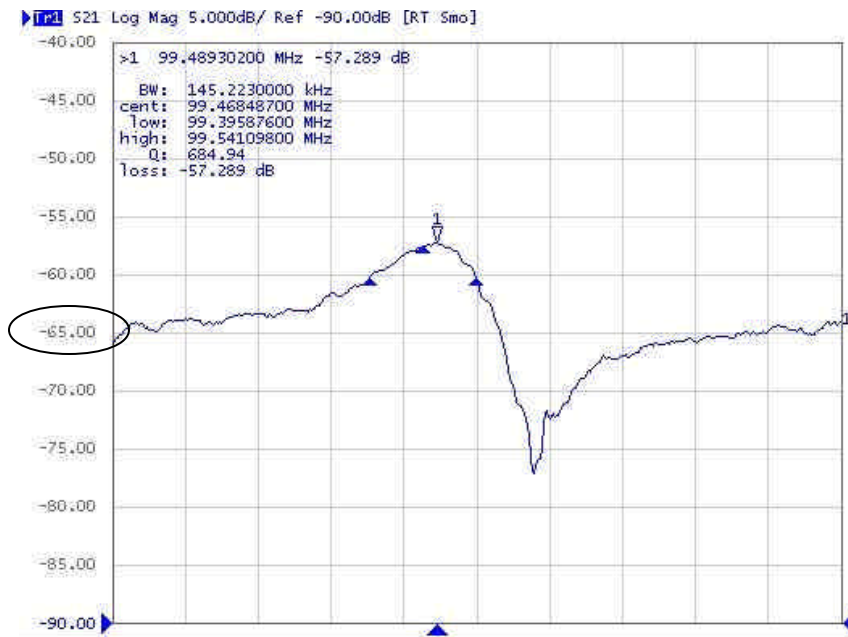


Fig. 4.13: At the 6th resonant mode in vacuum, after calibration. $Q=700$. Note the drop in the feed-through level (noise floor) from -26dB in fig. 4.10 to -65dB here.

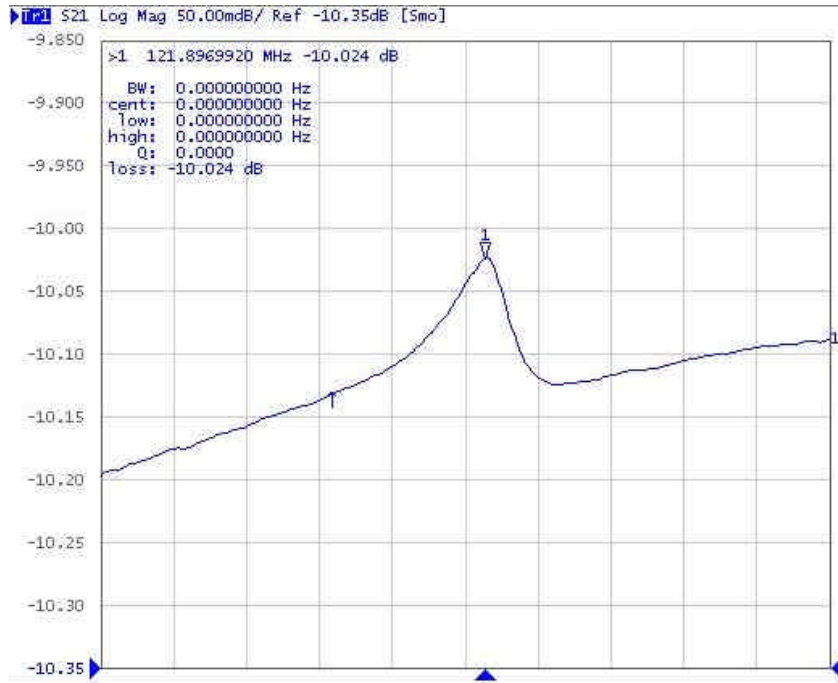


Fig. 4.14: At the 7th resonant mode in vacuum, $f = 121.89\text{MHz}$

120 μm by 30 μm block resonator

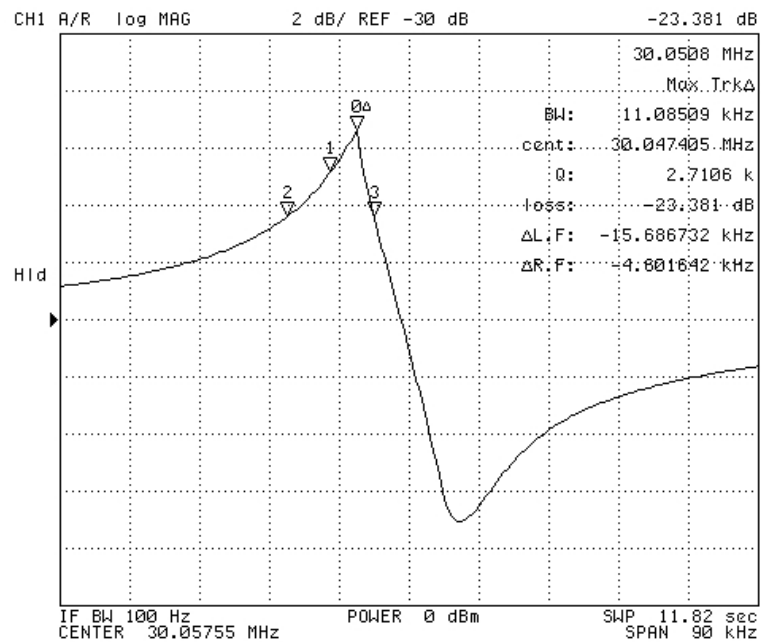


Fig. 4.15: At the fundamental resonant frequency in vacuum, $f = 30.05\text{MHz}$, $Q=2700$, power = 0dBm

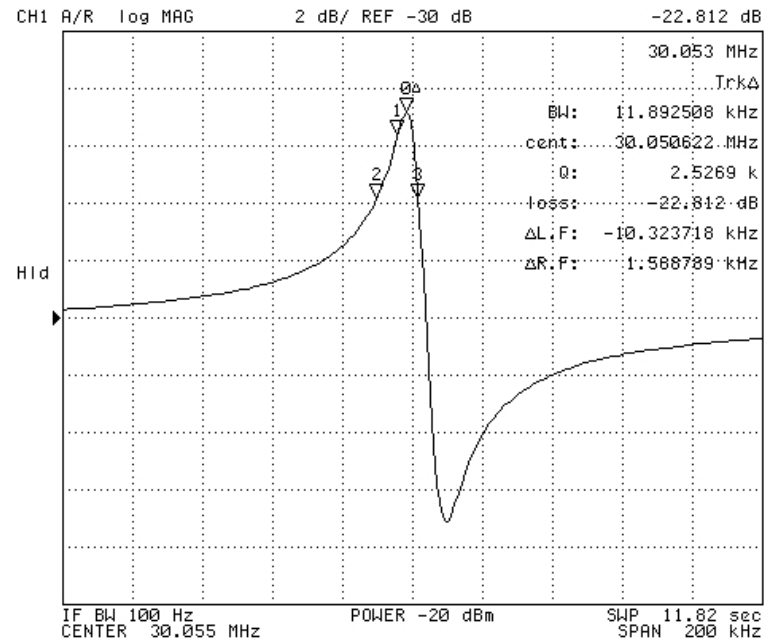


Fig. 4.16: At the fundamental resonant frequency in vacuum, $f = 30.05\text{MHz}$, $Q=2500$, power = -20dBm

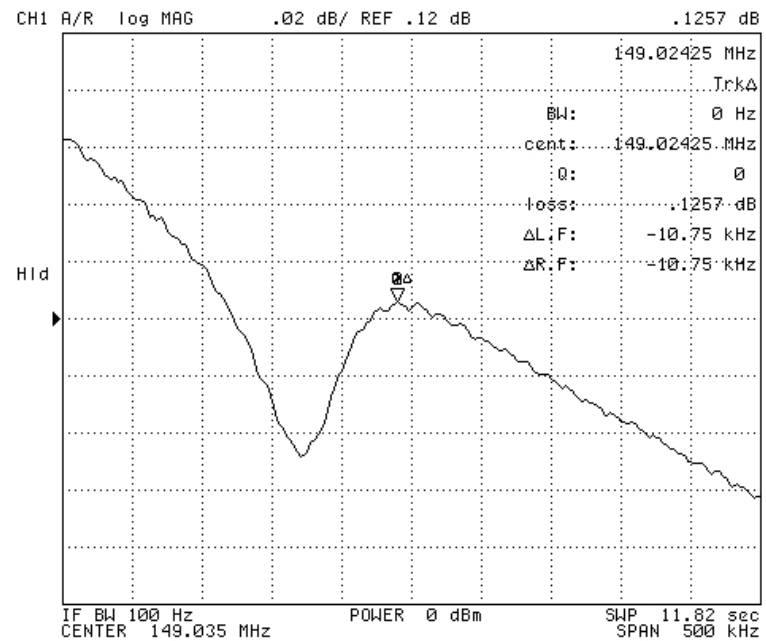


Fig. 4.17: At the 5th resonant mode in vacuum, $f = 149.02\text{MHz}$

40 μ m by 20 μ m block resonator

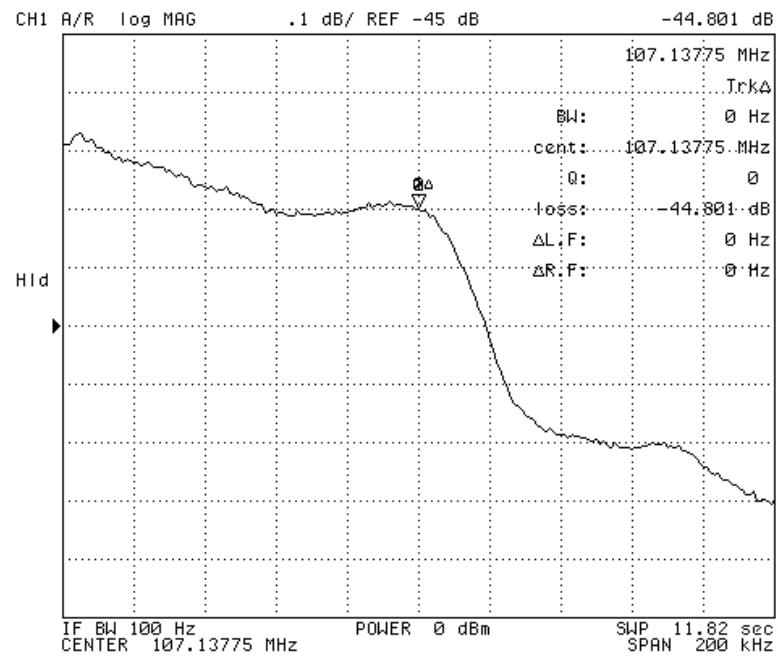


Fig. 4.18: At the fundamental resonant frequency in vacuum, $f = 107.14\text{MHz}$



Fig. 4.19: At the 3rd resonant mode in vacuum, $f = 323.26\text{MHz}$

It can be seen from the last plot that there are only bumps visible at these higher frequencies because the feed-through level is high. Proper calibration is required to cancel out the noise floor due to the feed-through to obtain peaks at these higher frequencies. However, without a low resistivity gold ground plane, even these bumps at high frequencies would not be visible.

CHAPTER 5

CONCLUSION AND FUTURE DIRECTIONS

This thesis reported on the fabrication and characterization results for piezoelectrically-transduced silicon micro-electro-mechanical resonators. The two piezoelectric materials taken into consideration were zinc oxide (ZnO) and lead-zirconate-titanate (PZT). Characterization of ZnO RF sputtering at an elevated temperature to obtain single crystalline films was performed. The need for a low resistivity ground plane for these devices was outlined, and steps were taken to successfully implement a gold ground plane on these devices. Reasonably good results were obtained from the ZnO-based devices, with small peaks observed at frequencies as high as 320MHz without any calibration of the feed-through.

A thorough literature review showed that PZT has superior piezoelectric properties when compared to ZnO, and can be used to enhance the frequency response of these resonators into the GHz range. However, incorporation of PZT is not a trivial task and therefore careful characterization of each layer forming the device was performed. RF sputtering of the PZT layer was thoroughly examined by altering all the parameters such as the sputtering power, the substrate-target distance, the sputtering pressure and the duration of deposition. As the as-sputtered layer was amorphous, a number of recipes for rapid thermal annealing of the PZT film were tried out. X-ray diffraction analysis was done for each set of sputtering and annealing parameters and an optimum recipe was identified for obtaining preferentially-oriented PZT thin films. All the experimentation had to be done taking into consideration the limitations of the RF sputterer and other equipment in the

clean room here. The top platinum electrode was also characterized and replaced with a gold/chrome electrode to avoid the use of negative resist which does now allow effective patterning of smaller features on the mask.

In spite of all this characterization, getting a successful batch of PZT-based resonators to work has still proved to be a challenge. Examination of each layer separately gives us optimum process parameters for that layer, but when all the layers are stacked to form the final device then there are delamination problems because of stress build-up in each layer. There has been ample proof of the PZT layer being strained, which is reflected in the shifted peaks in the XRD plots, as well as in SEM pictures taken after subjecting PZT to strong etchants. The top and ground electrodes come out shorted either because the PZT layer is too thin or because the delaminated portions break open when wire-bonded.

The primary layer in the device is the PZT layer, and the quality of this layer has to be extremely good and robust to get the resonators to work. The RF sputterer needs to be modified to allow for higher sputtering pressures up to 60mTorr, so that a tenacious thick film can be obtained with a smaller substrate-target distance. Also, incorporation of more adhesion layers is warranted. A titanium adhesion layer between PZT and platinum might prevent the delamination to some extent. This will however, reduce the quality factor of the resonator because additional layers will load the movable device even more. Bigger targets of PZT can also be used in the sputterer, with or without substrate heating. The larger the diameter of the target, the more power it can handle. Sputtering at a higher

power (90W to 110W) will give a much thicker film without the need for compromising the quality by reducing the substrate-target distance.

PZT has been shown to be an excellent piezoelectric material for incorporation into MEMS. Even though it involves exhaustive characterization at each level, it is definitely worth the effort. Referring back to the comparison between PZT and ZnO, it can be seen that the electromechanical coupling coefficient is almost 5 times larger for PZT. This means that the peaks observed in the network analyzer at any given frequency for PZT will be five times larger than that for ZnO, giving proportionally higher quality factors. This correlates to the fact that as we explore higher frequencies, instead of the small bumps we observed for ZnO-based devices, we will get well-defined peaks. Also, the higher feed-through level for PZT arising from its extremely large dielectric coefficient can be cancelled out by attaching an equally large inductance in parallel with it.

An effective calibration technique for testing piezoelectric resonators has not been developed till now, and there is potential for improvement in this area. The feed-through levels obtained without calibration are very high for these resonators because of the pad capacitances and other design issues. Some results with calibration in air have been provided in this thesis, but that is not an effective way to cancel out the noise. Two identical devices are required, one functional and one non-functional. Using the dummy device, the feed-through level should be identified and calibrated out during testing, and then the functional device should be tested under similar conditions to obtain a well-defined frequency response.

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